NEC

PRODUCT DESCRIPTION
VOICE RECOGNITION LSI SET
μPD7761
μPD7762

NEC ELECTRONICS (EUROPE) GMBH

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µPD7761

µPD7762

7/85 V1.0

VOICE RECOGNITION LSI SET

LOW-COST VERSION

μPD7761

μPD7762

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CHAPTER 1 VOICE RECOGNITION SYSTEM

The voice recognition LSI set (μPD7761D and μPD7762G) comprises all the main functions of a voice recognition system. A high-performance voice recognition system can be realized by interfacing the LSI set with a pattern registration memory and a host system. (If the special serial interface is used, no other interface is required.)

The primary functions of the LSI set are training (analysis of voice data and subsequent compression and storage of data) and recognition (comparing and verifying an input voice signal against the registered patterns and outputting the result based on a set of predetermined rules). The LSI set's functions can be controlled by simple commands issued from the host computer. This manual describes the specifications of a system adopting a general-purpose PCM CODEC for such voice signal preprocessing as filtering and A/D conversion.

1.1 Features

- Speaker dependent isolated word recognition system by the time compressed DP matching method.
- Word registration capacity: 128 words (with a 16K-byte basic memory) to 512 words (with a 64K-byte memory)
- Word length: 0.2 sec. - 2.0 sec. max.
- Grouping (Syntax control): 128 groups max.
- Recognition response time: 0.5 sec. on average
- Recognition accuracy: more than 95%
- A PCM CODEC (μ-law) can be used
- Three types of host interfaces
  1. Parallel interface using μPD8255A-5
  2. RS-232C interface using μPD8251AF
  3. Serial interface using μPD7762G serial port
- Four types of memory configurations available
  1. 16K bytes (basic configuration)
  2. 32K bytes
  3. 48K bytes
  4. 64K bytes (maximum)
- Simple command configuration using 11 types of commands

1.2 System Configuration

Figure 1-1 shows the basic configuration of a voice recognition system using the voice recognition LSI set (μPD7761D and μPD7762G). The system consists of the voice recognition LSI set and these four blocks.

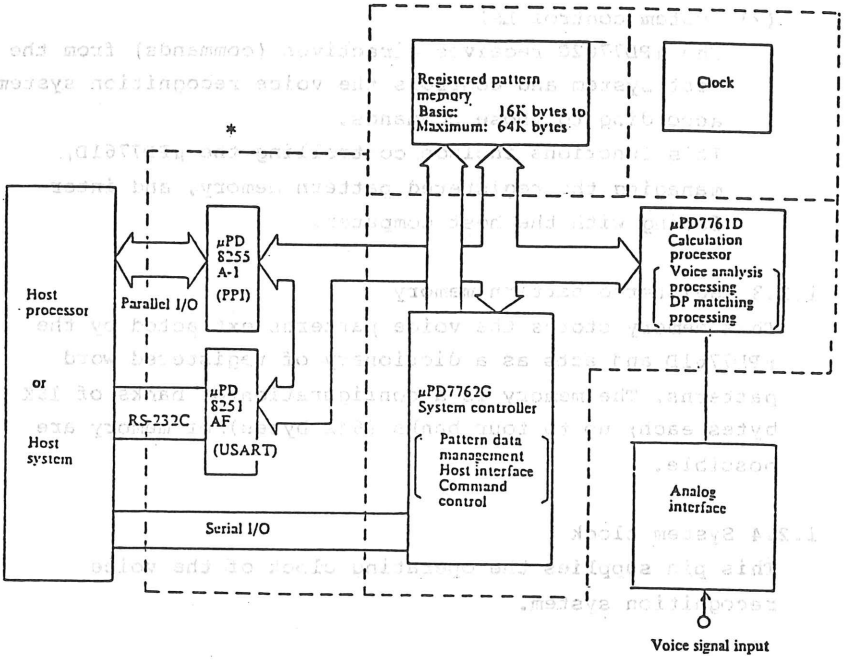
- Registered pattern memory
- System clock
- System interface
- Analog interface

1.2.1 Analog interface

After the analog voice signal (input from a mic, etc.) has been subject to bandpass filtering, it is converted to 8-bit digital data. In the circuit diagrams in this manual, a general-purpose PCM CODEC (μPD9513D or equivalent) has been adopted.

1.2.2 Voice recognition LSI set

The heart of the voice recognition system is these LSIs that function as the calculation processor and the system controller.



* One of the three available I/O interfaces should be selected.

Fig. 1-1 System Configuration

(1) Calculation processor

The μPD7761D is an LSI used exclusively for such calculations as voice analysis and DP matching. To perform voice analysis, the voice pattern is extracted from the signals input from the analog interface (digital voice data), using an eight-channel digital filter.

An eight-bit data bus connects the μPD7761D to the μPD7762G. This bus transfers voice analysis data, pattern data required for DP matching, and the result of the matching between the μPD7761D and the μPD7762G.

(2) System control LSI

The μPD7762G receives directives (commands) from the host system and controls the voice recognition system according to those commands.

It's functions include controlling the μPD7761D, managing the registered pattern memory, and interfacing with the host computer.

1.2.3 Registered pattern memory

This memory stores the voice patterns extracted by the μPD7761D and acts as a dictionary of registered word patterns. The memory is a configuration of banks of 16K bytes each; up to four banks (64K bytes) of memory are possible.

1.2.4 System clock

This pin supplies the operating clock of the voice recognition system.

1.2.5 System interface

This is the interface between the host system and the voice recognition system. Three interfaces are available.

(1) Parallel

(2) RS-232C

(3) Serial

CHAPTER 2 VOICE RECOGNITION SYSTEM CONFIGURATION EXAMPLE

2.1 Analog Interface

The analog interface converts the voice signal input from a microphone or similar source to 8-bit digital data for input to the μPD7761D. The circuit is configured of a mic amp, ALC (automatic level control) and a PCM CODEC. A circuit configuration example is shown in Fig. 2-1.

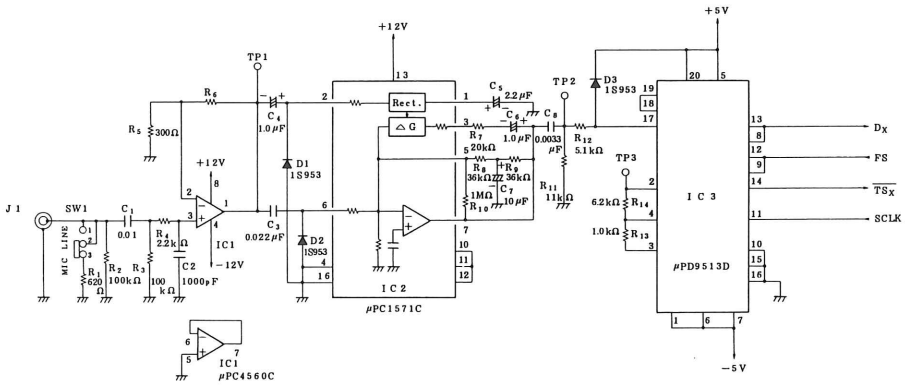


Fig. 2-1 Circuit Example for the Voice Recognition LSI Set

2.1.1 Mic Amp

The output voltage of the microphones is normally very small (from several ten μV to several mV), requiring the use of a mic amp. In the example in Fig. 2-1, an operational amplifier μPC4560C IC1 is used as the mic amp. The voltage gain (Av) can be set by the the ratio of resistances R5 and R6 as shown in the following formula.

$$Av = 1 + \frac{R6}{R5}$$

C1 and R3 form a filter that suppresses low-frequency noise such as the power supply hum, and C2 and R4 a filter that eliminates high frequencies.
Use of a microphone, such as a close-talking type, that will not pick up surrounding noise is recommended.
Impedance should be 1KΩ max.

2.1.2 ALC circuit

In the example in Fig. 2-1, a μPC1571C (IC2) is used as an ALC circuit.

2.1.3 PCM CODEC

The following circuits are required to perform analog-digital conversion of the input signals.

Bandpass filter	To suppress distortion introduced by the sampling clock
Sample and hold	To digitalize data in the time axis direction
A/D converter	To digitalize data in the amplitude direction

A general-purpose PCM CODEC (μPD9513D, 9514D, 9516D, 9517D, etc.) will provide all of these functions. Fig. 2-2 shows a block diagram of the μPD9513D.

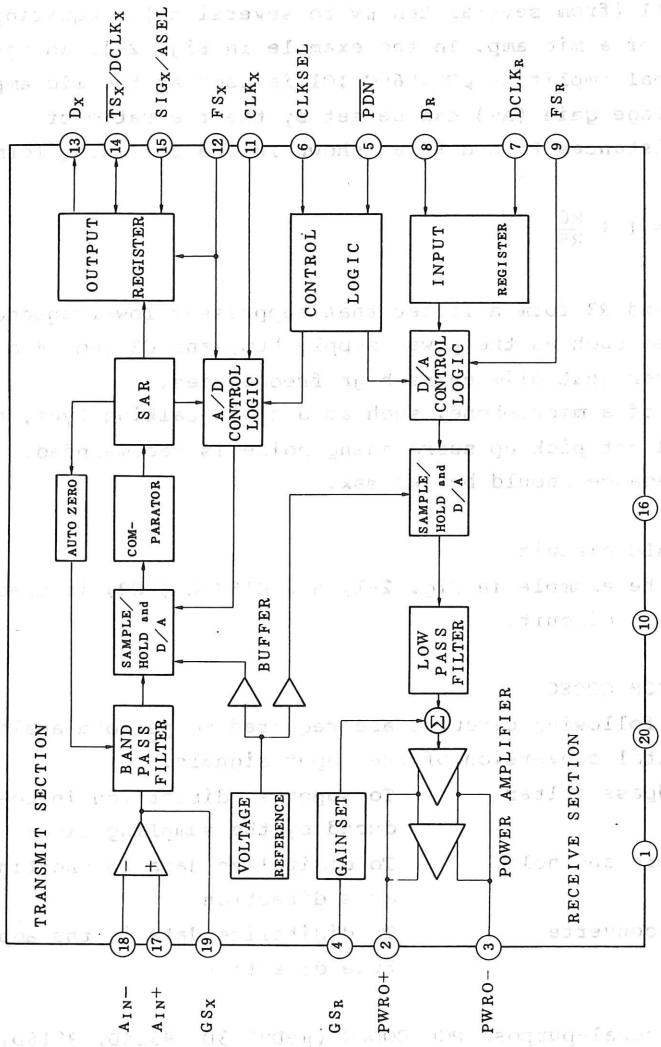
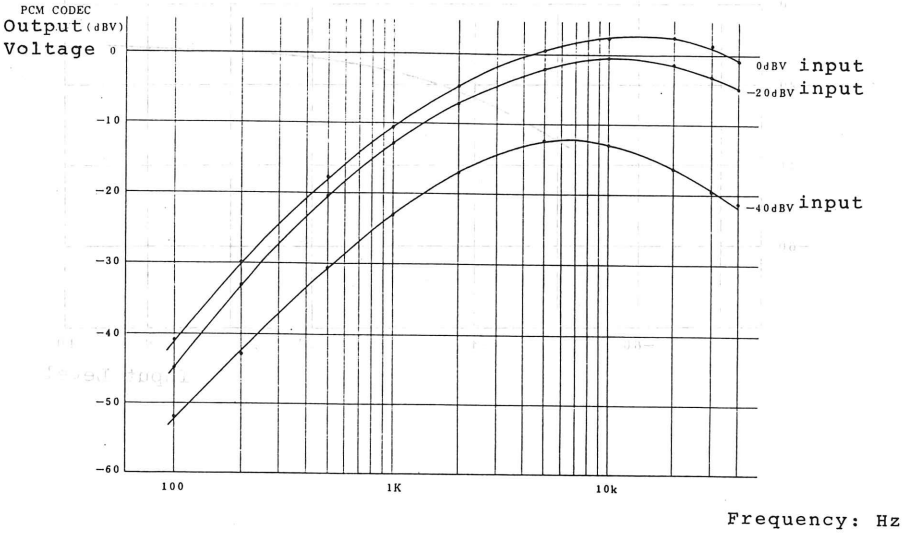


Fig. 2-2 μPD9513D Block Diagram

Figs. 2-3 and 2-4 show the characteristics for the analog interface.



Note: Mic amp gain: 0dB

Fig. 2-3 Mic Input vs PCM CODEC Input Frequency

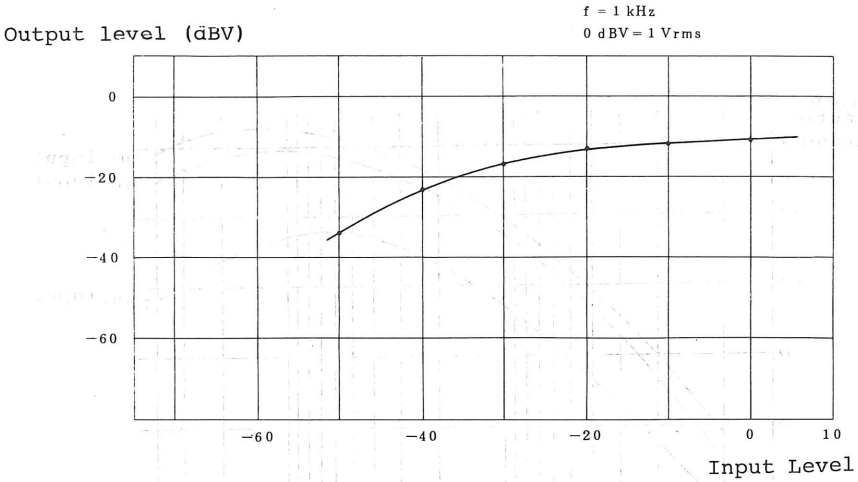


Fig. 2-4 Mic Input vs PCM CODEC Input Level

2.2 Voice Recognition LSI Set

2.2.1 μPD7761D/PCM CODEC interface

The μPD7761D (calculation processor) has an on-chip serial interface for input of digitial voice data. The format for this data is shown in Table 2-1(a). Here it can be seen that the coding used is natural binary coding as per A-law (recommended in CCITT G.711) and that alter bit processing is not performed.

Note that A-law format PCM CODECs such as the μPD9513D, 9514D, 9517D, etc. perform alter bit processing. Therefore, when such a device is interfaced with a μPD7761D, alter bit processing of the PCM CODEC output must again be performed. (See Table 2-1(b).)

In the case of a μ-law format PCM CODEC (μPD9513D, 9514D, 9516D, etc.) the output data is inverted, enabling easy interfacing.

However, even though the polarity bit data is also inverted, because the negative/positive waveforms of a voice signal are almost symmetrical, this presents no obstacle in terms of application. (See Table 2-1(c).)

Note:

Alter bit processing refers to the type of processing in which the even-numbered bits of data are inverted.

Table 2-1 μPD7761D and PCM CODEC Coding Formats

(a) μPD7761D input code

	Seg	Output data 1 2 3 4 5 6 7 8
+FS		1 1 1 1 1 1 1 1
	7	1 1 1 1 1 0 0 0
	6	1 1 1 0 0 0 0 0
	5	1 1 0 1 0 0 0 0
	4	1 1 0 0 0 0 0 0
	3	1 0 1 1 0 0 0 0
	2	1 0 1 0 0 0 0 0
	1	1 0 0 0 0 0 0 0
0		0 0 0 0 0 0 0 0
	1	0 0 0 0 0 0 0 0
	2	0 0 1 0 0 0 0 0
	3	0 0 1 1 0 0 0 0
	4	0 1 0 0 0 0 0 0
	5	0 1 0 1 0 0 0 0
	6	0 1 1 0 0 0 0 0
	7	0 1 1 1 0 0 0 0
-FS		0 1 1 1 1 1 1 1

(b) μPD9513,9514D, 9517D (A-law) output code

	Seg	Input data 1 2 3 4 5 6 7 8
+FS		1 0 1 0 1 0 1 0
	7	1 0 1 0 0 1 0 1
	6	1 0 1 1 0 1 0 1
	5	1 0 0 0 0 1 0 1
	4	1 0 0 1 0 1 0 1
	3	1 1 1 0 0 1 0 1
	2	1 1 1 1 0 1 0 1
	1	1 1 0 1 0 1 0 1
0		0 1 0 1 0 1 0 1
	1	0 1 0 1 0 1 0 1
	2	0 1 1 1 0 1 0 1
	3	0 1 1 0 0 1 0 1
	4	0 0 0 1 0 1 0 1
	5	0 0 0 0 0 1 0 1
	6	0 0 1 1 0 1 0 1
	7	0 0 1 0 0 1 0 1
-FS		0 0 0 1 0 1 0 1

(c) μPD9513D,9514D 9516D (μ-law) output code

	Seg	Output data 1 2 3 4 5 6 7 8
+FS		1 0 0 0 0 0 0 0
	8	1 0 0 0 1 1 1 1
	7	1 0 0 1 1 1 1 1
	6	1 0 1 0 1 1 1 1
	5	1 0 1 1 1 1 1 1
	4	1 1 0 0 1 1 1 1
	3	1 1 0 1 1 1 1 1
	2	1 1 1 0 1 1 1 1
	1	1 1 1 1 1 1 1 1
0		0 1 1 1 1 1 1 1
	1	0 1 1 1 1 1 1 1
	2	0 1 1 0 1 1 1 1
	3	0 1 0 1 1 1 1 1
	4	0 1 0 0 1 1 1 1
	5	0 0 1 1 1 1 1 1
	6	0 0 1 0 1 1 1 1
	7	0 0 0 1 1 1 1 1
	8	0 0 0 0 1 1 1 1
-FS		0 0 0 0 0 0 0 0

When a μPD9513D operating in μ-law is used as the PCM CODEC, the interface circuit should be as shown in Fig. 2-5 and the clock timing as shown in Fig. 2-6.

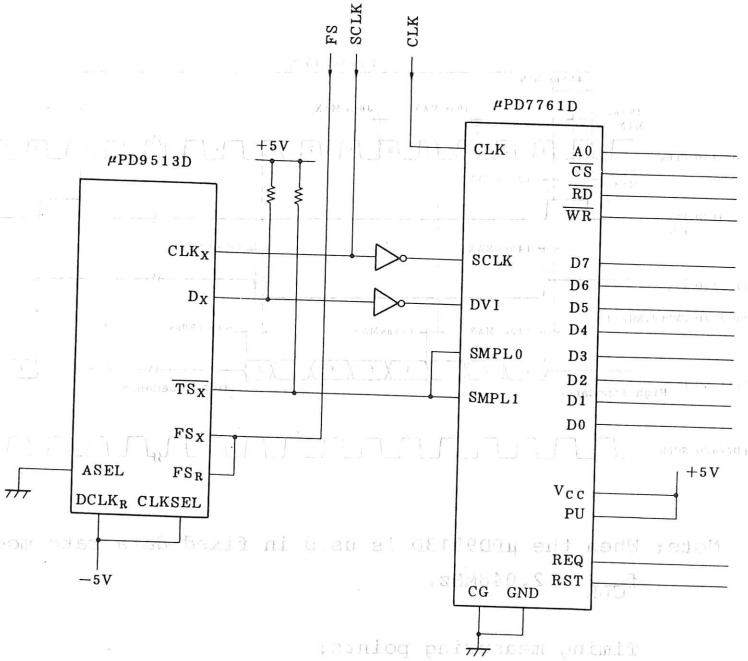
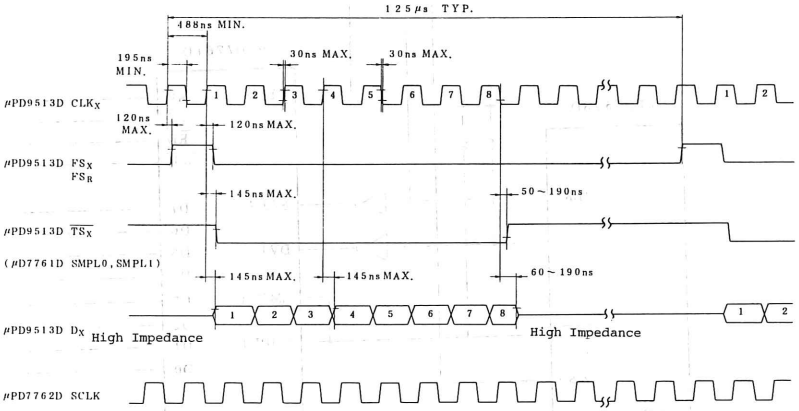


Fig. 2-5 Interface Circuit for μPD9513D (μ-law)



Note: When the μPD9513D is used in fixed data rate mode, f_{CLK} = 2.048MHz.

Timing measuring points:

Low level : 0.8V

High level : 2.0V

Fig. 2-6 Interface Clock Timing

2.2.2 μPD7761D and μPD7762G interface

A connection example for the μPD7761D and the μPD7762G is shown in Fig. 2-7.

The μPD7762G initializes the voice recognition system when power is applied. These are the conditions at initialization:

- Level flags are reset for all memory banks set by the MM0 and MM1 pins of the μPD7762G. (The level flags are set by executing the LEVEL ADJUST command.)
- The current bank is set to bank 0.
- All system interfaces are initialized. At this time, even if one or more interfaces are not connected, no error will occur.
- The μPD7761D is reset.

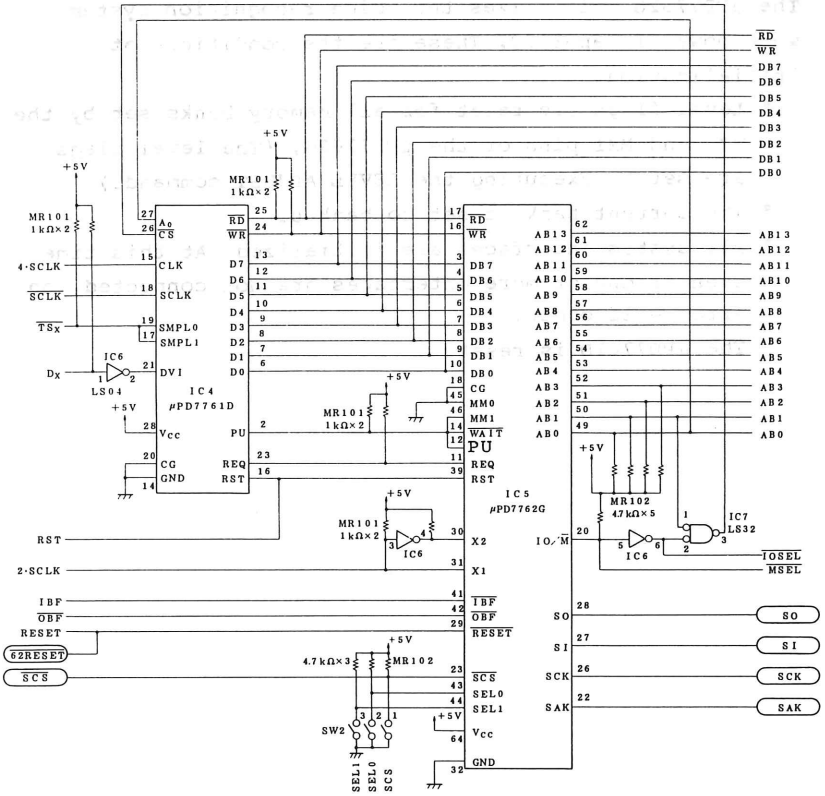


Fig. 2-7 μPD7761 / μPD7762 Connection Example

2.3 Registered Pattern Memory

The registered pattern memory is a configuration of 16K-byte banks; a maximum of 64K bytes can be mounted (see Fig. 2-8). The memory capacity is specified by the state of the MM0 and MM1 pins of the μPD7762G (see Table 2-1).

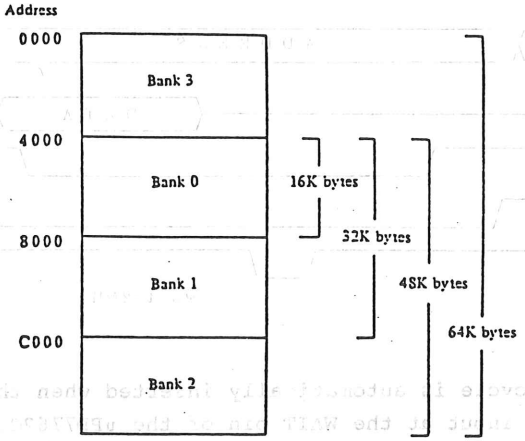


Fig. 2-8 Memory Bank Configuration

Table 2-2 Setting Memory Capacity

MM0	MM1	Memory size
L	L	64K bytes
L	H	16K bytes
H	L	32K bytes
H	H	48K bytes

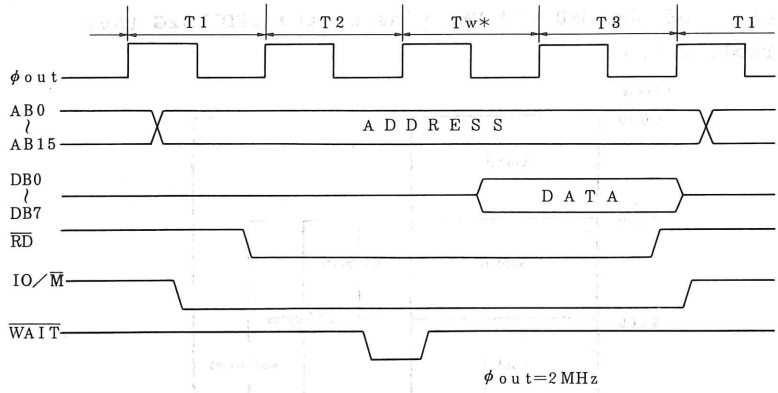
H: High level
L: Low level

2.3.1 Read cycle

Figure 2-9 shows the timing for the memory read signal output from the μPD7762G.

Note that a wait cycle is included in the read cycle timing. This is because when a 4MHz clock is input as the operating clock of the μPD7762G, the access time is only 350ns. This means that to use a dynamic RAM, the read operation must include a wait cycle. Insertion of a wait cycle extends the access time to 850ns, enabling use of almost any dynamic RAM.

An example of this type of wait signal generating circuit is shown in Fig. 2-9.



* One wait cycle is automatically inserted when the wait signal is input at the WAIT pin of the μPD7762G.

Fig. 2-10 μPD7762 Memory Read Timing

μPD7762G Output

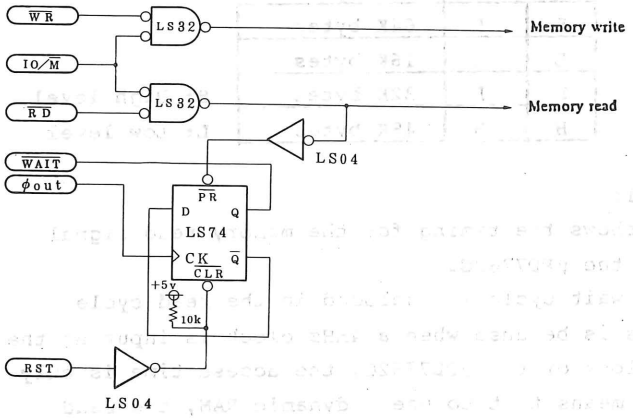


Fig. 2-10 Example of a Circuit to Generate One Wait Signal During Memory Read

The μPD7762G senses the wait signal during the T2 state. If the signal is low, it automatically inserts a wait cycle (T_W).

At the end of T_W, the wait pin is sensed; if it is low, another wait cycle is inserted. TW will repeat as long as the wait signal is low.

2.3.2 Write cycle

Figure 2-11 shows the timing of the memory write signal output from the μPD7762G.

The write cycle differs from the read cycle in that no wait cycle is required. Because when a 4MHz clock is used, a WR signal width of 600ns is assured and a normal RAM will latch the data at the trailing edge of the WR signal.

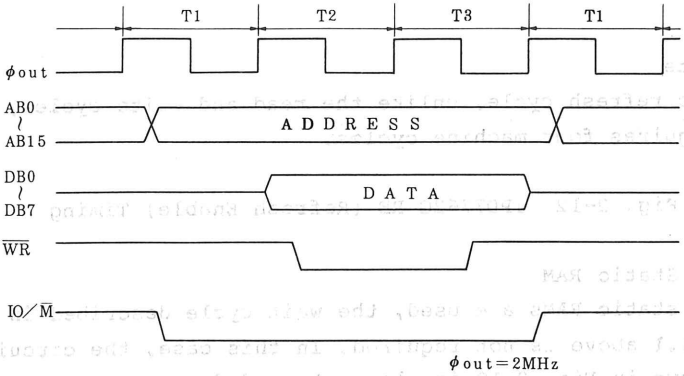
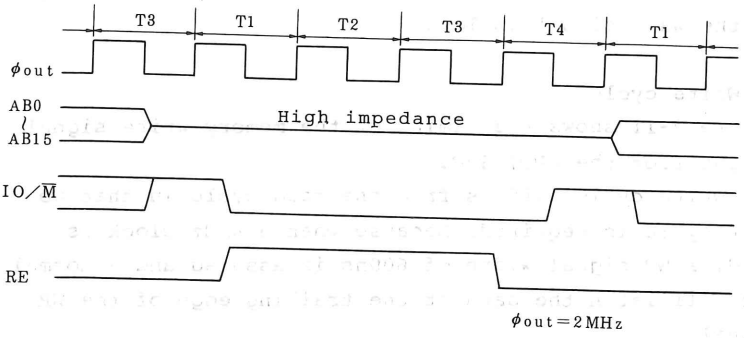


Fig. 2-11 μPD7762G Memory Write Timing

2.3.3 Refresh cycle

Because cases may occur in which a dynamic RAM is used for the registered pattern memory, the μPD7762G is provided with a refresh enable (RE) pin in addition to the wait input (WAIT) pin discussed above. Figure 2-12 shows the timing for the RE pin. When the μPD7762G is not performing memory access, the RE pin outputs a high-level signal; at the same time, the IO/$\overline{M}$ pin outputs a low-level

signal. At this time, the address bus of the μPD7762G is held at high impedance.



Note

The refresh cycle, unlike the read and write cycles, requires four machine cycles.

Fig. 2-12 μPD7762G RE (Refresh Enable) Timing

2.3.4 Static RAM

If static RAMs are used, the wait cycle described in 2.3.1 above is not required. In this case, the circuit shown in Fig. 2-10 is also not needed.

The wait pin of the μPD7762G should be pulled up by a resistance of about 10KΩ. Fig. 2-8 shows a circuit example for a registered pattern memory using static RAMs.

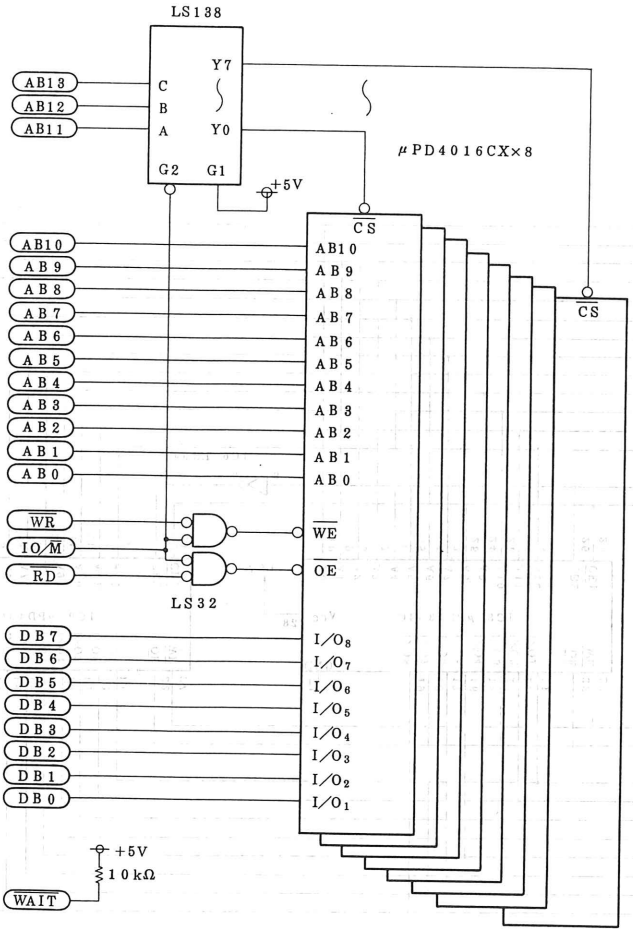


Fig. 2-13(a) Memory Configuration Using Static RAMs (μPD4016 (16K bit))

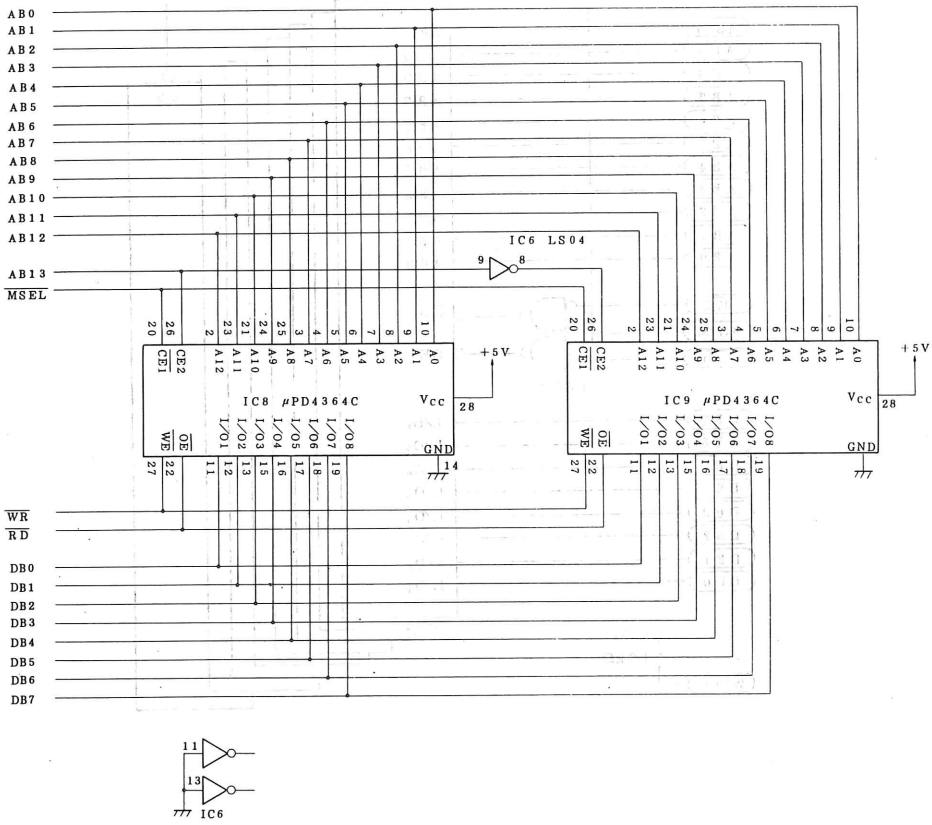


Fig. 2-13(b) Memory Configuration Using Static RAMS (μPD4346C (64K bit))

2.4 System Clocks

The system clocks required by the voice recognition system are given in Table 2-3.

Table 2-3 Clock Signals to be Supplied to the Voice Recognition LSI Set

Device	Frequency	Supply pins	Notes
μPD7761D	8.192MHz	CLK	μPD7761D master clock
	2.048MHz	SCLK	Serial input clock
	8.0kHz	SMPL0,SMPL1	Sampling clocks
μPD7762G	4.096MHz	X1,X2	μPD7762G master clock
μPD9513D (PCM CODEC)	2.048MHz	CLK_X,CLK_R	μPD9513D master clock, serial transmit clock; inverse phase of SCK of μPD7761D
	8kHz	FS_X,FS_R	Frame cycle clock; same clock as SMPL0,SMPL1 of μPD7761D can be used

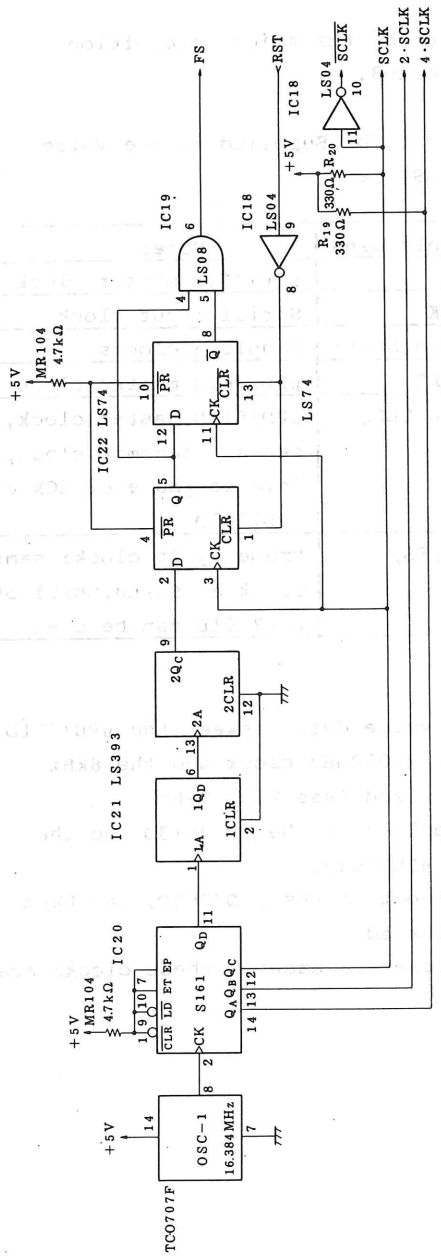
Notes concerning clocks

(1) When sending digital voice data between the μPD7761D and the μPD9513D, the 2.098MHz clock and the 8kHz clock must be synchronized (see Fig. 2-6).

(2) The 8kHz clock is supplied to the μPD9513D and the inverse phase to the μPD7761D.

(3) When reset (RST) is input to the μPD7761D, the 8kHz clock must also be cleared.

Examples of circuits to generate each of these clocks are shown in Fig. 2-14.



(注) IC18のピン13はGNDに接続
IC19のピン9,10,12,13はGNDに接続

Fig. 2-14 Clock Generation Circuit Example

2.5 System Interface

Three different types of system interfaces can be used with the voice recognition LSI set. By using these interfaces, data communication with the host system can be performed in 8-bit units.

The host interface is managed by the μPD7762G. These three types of interfaces are supported:

(1) Parallel interface (μPD8255A-5)

(2) RS-232C interface (μPD8251AF)

(3) Serial interface (serial port of the μPD7762G)

Table 2-4 Interface Selection

SEL0	SEL1	Interface
L	L	μPD8255A-5 parallel
L	H	μPD7762G serial
H	L	Use prohibited
H	H	μPD8251AF RS-232C

H: High level
L: Low level

2.5.1 Parallel interface (μPD8255A-5)

The host system performs 8-bit parallel data communication via the μPD7762G and the μPD8255A-5. The μPD8255A-5 is supported as a peripheral device of the host. The bits of group A should therefore be set in mode 2. The bits of group B can be set in any mode.*

Fig. 2-15 shows how to connect the μPD8255A-5 and the μPD7762G.

As can be seen in the figure, the input signals for μPD8255A-5 pins $\overline{ACK}$ and $\overline{STB}$ are generated by μPD7762G outputs IO/M, AB2 (active low) and RD/WR.

Also, the outputs of μPD8255A-5 pins $\overline{OBF}$ and IBF are input without change to μPD7762G pins $\overline{OBF}$ and IBF.

Fig. 2-16 shows a circuit example when a μPD8085A is used as the host.

* The μPD8255A-5 is provided with three 8-bit ports referred to as ports A, B, and C. Bits 4 to 7 of port C

in combination with all port A bits are called group A, and bits 0 to 3 of port C in combination with all port B bits are called group B. The port C bits in these configurations can be used for output of control signals or input of status signals.

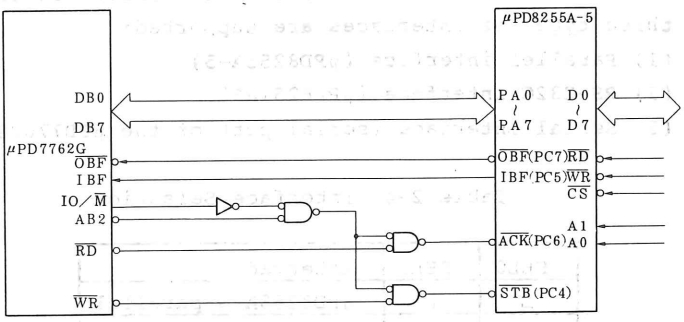


Fig. 2-15 Parallel Interface

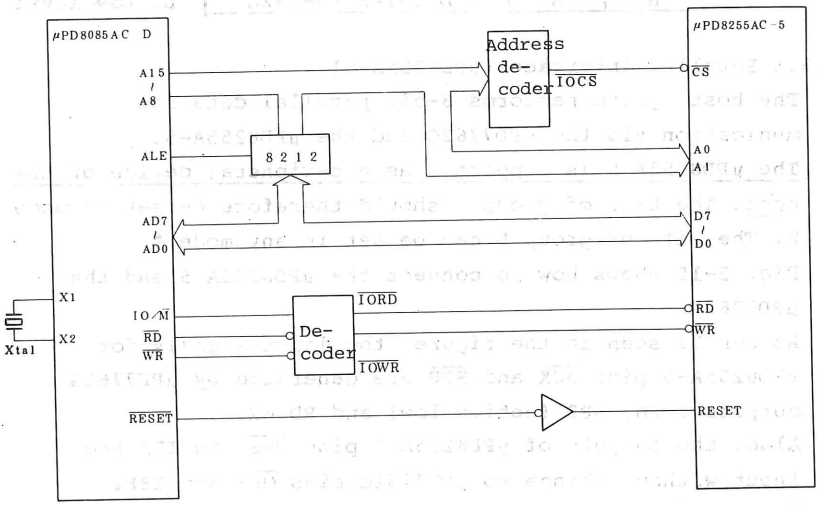


Fig. 2-16 Connecting μPD8085AC/D(-2) and PPI (μPD8255AC-5)

Notes on reset

The reset signal sent to the μPD7762G must be held at low level until the system completes the mode setting of the μPD8255A-5. This prevents any misoperation. It is not necessary when the serial or RS-232C is used for the host interface.

Figure 2-17 shows a circuit example used to perform this reset operation. In this circuit, the reset signal rises after the initial write (of the mode setting code) has been received from the host system.

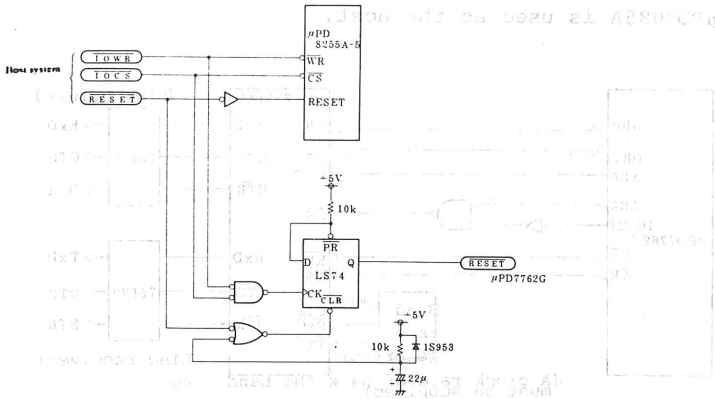


Fig. 2-17 Reset Signal Synchronization Circuit

2.5.2 RS-232C interface (μPD8251AF)

When a μPD8251AF (USART) is used as the host interface, the host system communicates with the μPD7762G in 8-bit units using the RS-232C communication standard. The μPD8251AF is supported as a peripheral device of the μPD7762G. Another μPD8251AF must therefore be provided on the host side.

Figure 2-18 shows a connection example of a μPD7762G and μPD8251A.

As the figure shows, the $\overline{CS}$ signal of the μPD8251AF is generated by the AB3 and IO/$\overline{M}$ signals of the μPD7762G, and the AB0 signal of the μPD7762G is used as the C/$\overline{D}$ signal of the μPD8251AF.

The μPD7762G sets the μPD8251AF in the mode shown below. The mode and the setting at the host side must conform.

- μPD8251AF operation mode specification: (mode setting data= 0CFH)
  1. Clock rate: baud rate x 64 (maximum baud rate=4800) (when CLK=2MHz)
  2. Word length: 8 bits
  3. Parity: disabled (no parity)
  4. Stop bits: 2 bits
  5. Communication mode: asynchronous

Fig. 2-19 shows an example of a circuit in which a μPD8085A is used as the host.

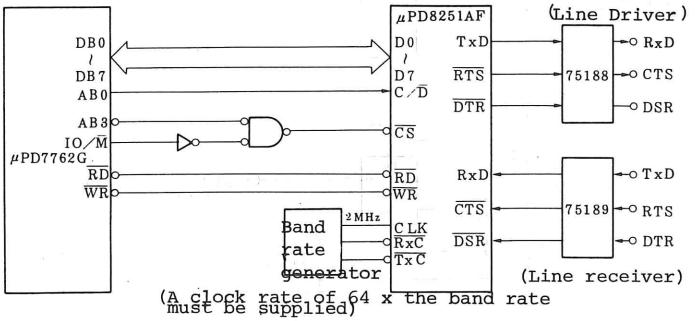


Fig. 2-18 Connection of μPD8251AF (μPD8251AF also supported as peripheral of the host)

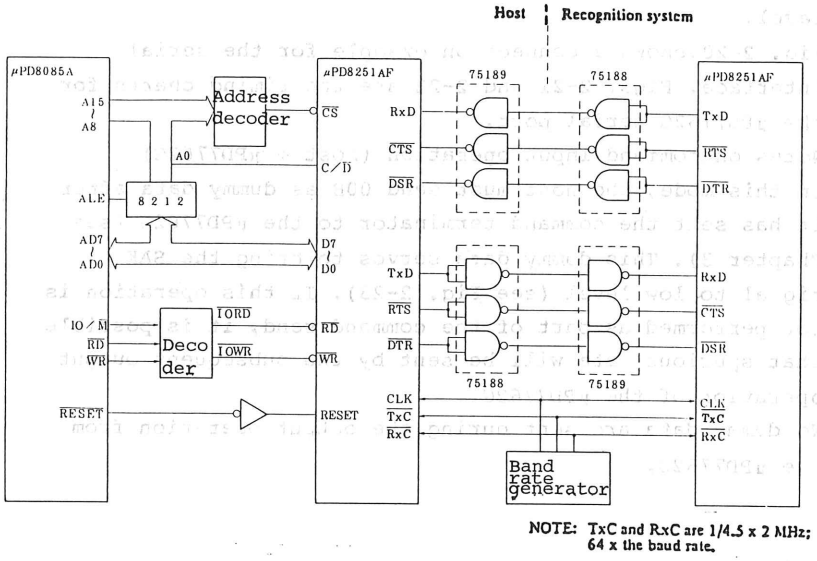


Fig. 2-19 Connection of μPD8085A(-2) and USART (μPD8251AF)

2.5.3 μPD7762G serial port interface

The μPD7762G incorporates a port capable of performing serial I/O. Eight-bit data communication is therefore possible with a host system having a port with the same timing.

The serial I/O clock SCK is supplied from the host. In this mode, when I/O operation completion is detected, the μPD7762G issues a low level SAK signal as confirmation. When all the 8-bit data have been input or output from the serial register of the μPD7762G, this SAK signal will go low (a in Figs. 2-21 and 2-22).

Likewise, when internal data are fetched from the serial register of the μPD7762G or when data are written to this register, the SAK signal goes high (b in Figs. 2-21 and 2-22).

The host system therefore performs data I/O after confirming that the SAK signal has risen from low to high level.

Fig. 2-20 shows a connection example for the serial interface. Figs. 2-21 and 2-22 are the timing charts for the μPD7762G serial port.

Notes on command input operation (host → μPD7762G)

In this mode, the host must send 00H as dummy data after it has sent the command terminator to the μPD7762G (see Chapter 3). This dummy data serves to bring the SAK signal to low level (see Fig. 2-23). If this operation is not performed as part of the command send, it is possible that spurious data will be sent by the subsequent output operation of the μPD7762G.

No dummy data are sent during the output operation from the μPD7762G.

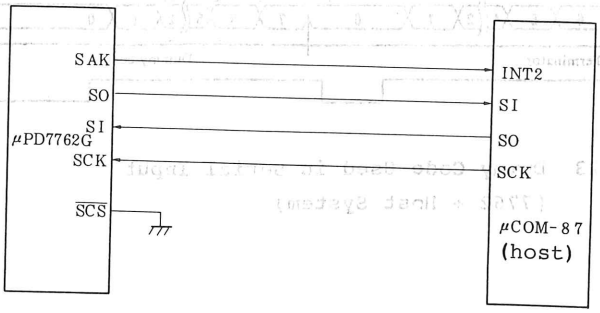


Fig. 2-20 Connection of the μPD7762G Serial Port

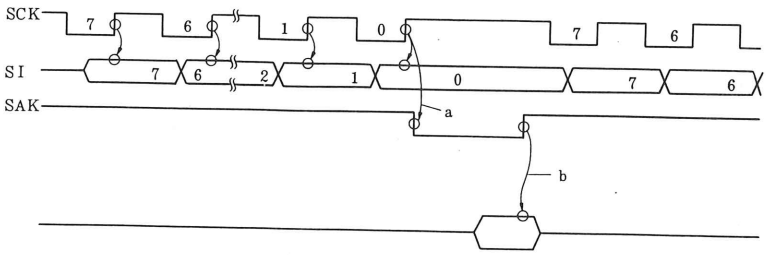


Fig. 2-21 μPD7762G Serial Input (7762 ← Host System)

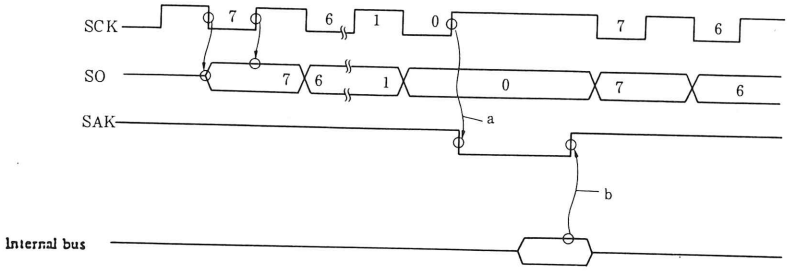


Fig. 2-22 μPD7762G Serial Output (7762 → Host System)

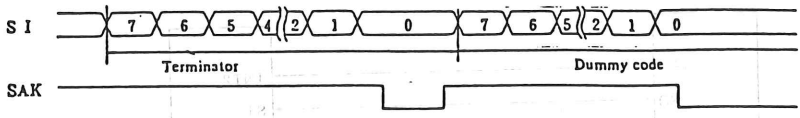


Fig. 2-23 Dummy Code Used in Serial Input (7762 + Host System)

CHAPTER 3 COMMANDS

The host system sends commands to the voice recognition system to control its operation.
Commands consist of the command code (8-bit binary code), the required parameters, and the terminator code (0FFH).

3.1 Command Format

The μPD7762G is provided with the 11 types of commands shown in Table 3-1. These commands can further be divided into four separate categories (Table 3-1 and Fig. 3-1).

Table 3-1 Types of Commands

Command Name	Command Format
INITIALIZE	00H,0FFH
LEVEL ADJUST	01H,[bank No.][bank No.][bank No.][bank No.],0FFH
TRAINING	02H,registration No.,[syntax No.,word reject value],0FFH
RECOGNITION	03H,[syntax No.][...][syntax No.],0FFH
SECOND DECISION	04H,0FFH
DOWN LOAD	06H,No. of patterns,0FFH
UP LOAD	07H,0FFH(used as a pair with DOWN LOAD command)
CHANGE BANK REJECT	08H,bank reject value,0FFH
MEMORY TEST	09H,0FFH
BANK SELECT	0AH,bank No.,0FFH
CHANGE WORD REJECT	0CH,registration No.,word reject value,0FFH

Notes

0FFH is the terminator.

Items enclosed in brackets can be omitted.

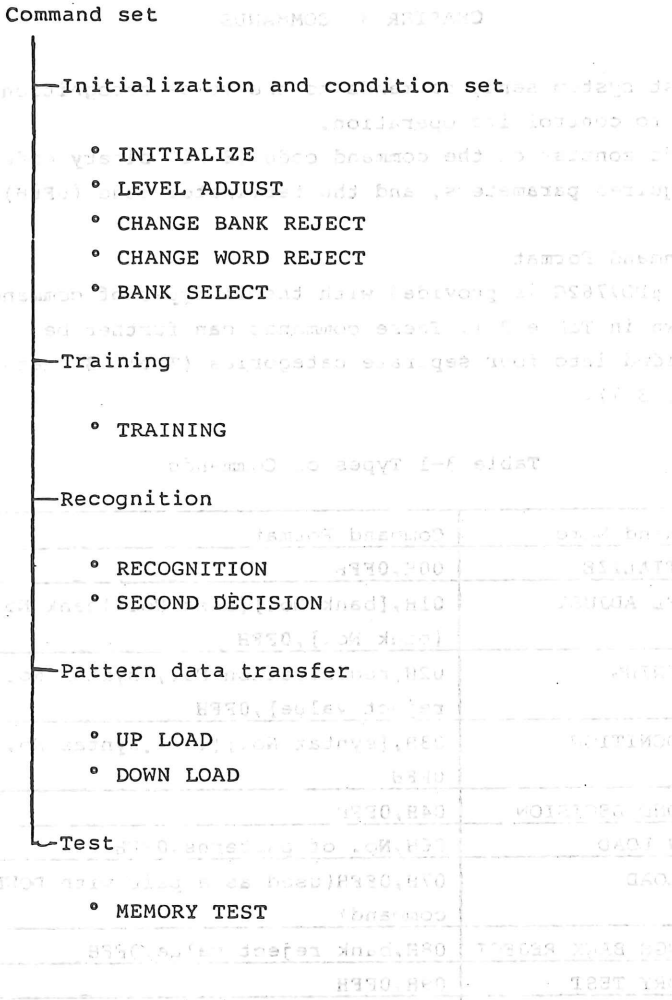


Fig. 3-1 Organization of Voice Recognition LSI Set Commands

3.2 Two Chip Voice Recognition Commands

When a general-purpose PCM CODEC is used for the analog interface instead of the MC4760, the LEVEL ADJUST command becomes unnecessary.

3.2.1 Bypassing the LEVEL ADJUST command

In the two-chip recognition LSI system, after the INITIALIZE command is executed, the LEVEL ADJUST command must be bypassed. The follows description shows how this is done.

Procedure

(1) Write FFD4H followed by FFH.

(2) Write 70CD followed by a two byte "noise data" (corresponding to the ambient noise level).

Table 3-2 Noise Data

Ambient noise	Data
50dB(A)	0040 to 0100H
60dB(A)	0080 to 0200H

Transfer data format:

0EH, D0H, 04H, F0H, 0FH, 00H, 01H, 00H, 00H, FFH, FFH, (FFD4 followed by FFH)

If the result status is 00H, perform the following process:

0EH, C0H, 0DH, 70H, 00H, 00H, 02H, 00H, 00H, FFH, [DL], [DH], (70CDH followed by 2-byte noise data)

Noise data should be written 1 byte at a time, in the order of the low- and the high-order bytes.

3.3 Commands

In the command descriptions that follow, items enclosed in brackets can be omitted.

3.3.1 Initializaton and condition set

(1) INITIALIZE (2 bytes)

Format : 00H,0FFH

Function : Initializes the voice recognition system while maintaining the current state of the system interface.

- Resets the μPD7761D.
- Initializes the reject value for the current bank of the registered pattern memory.
  (Word reject value=0FEH)
  (Bank reject value=0AH)

Status : 00H (normal completion)

output 09H (command format error)

(2) LEVEL ADJUST (2 to 6 bytes)

Format : 01H,[Bn],[Bn],[Bn],[Bn],0FFH

$00H \leq Bn \leq 03H$

Bn: Bank number

Function : Calibrates the ATC values of the MC-4760. This command must be executed after power is ON or when the INITIALIZE command has been executed.

- A voice signal is input and the ATC values are adjusted to obtain an appropriate input level.
- Resets the level flags of the specified memory banks.
- If the memory bank specification is omitted, level flags for all the banks selected by the condition of the MM0 and MM1 pins of the μPD7762G and bank 0 will be set as the current bank.

Status : 00H (normal completion)
output 08H (specified bank does not exist)
09H (command format error)
01H (input voice level too high)
02H (input voice level too low)

(3) CHANGE BANK REJECT (3 bytes)

Format : 08H,reject value,0FFH
00H ≤ reject value ≤ 0FEH

Function : Changes the reject value of the current memory bank.

Status : 00H (normal completion)
output 09H (command format error)

(4) CHANGE WORD REJECT (4 bytes)

Format : 0CH,registration No.,reject value,0FFH
01H ≤ registration No. ≤ 80H
00H ≤ reject value ≤ 0FEH

Function : Changes the reject value for words that have already been registered.

Status : 00H (normal completion)
output 09H (command format error)
↑
This error code will be output if a registration number above 80H is specified.

(5) BANK SELECT (3 bytes)

Format : 0AH,bank No.,0FFH
00H ≤ bank No. ≤ 03H

Function : Selects the specified memory bank

Status : 00H (normal completion)
output 08H (specified bank does not exist)
09H (command format error)

(6) HOT START (2 bytes)

Format : 05H,0FFH

Function : Initializes the voice recognition system while maintaining the registration patterns in memory.
This command is used when the system interface has been changed or when the system stops operating because of error.
- Initializes the host interface.
- Resets the μPD7762G.

Status output : 00H (normal completion)
09H (command format error)

3.3.2 Training

(1) TRAINING (3 to 5 bytes)

Format : 02H,registration No.,[syntax No.,reject value],0FFH
01H ≤ registration No. ≤ 80H
00H ≤ syntax No. ≤ 80H (if omitted, 0)
00H ≤ reject value ≤ 0FEH (if omitted, 0FEH)
If one of the above two parameters is omitted, they both should be omitted.

Function : Performs registration of voice patterns.
- Analyzes input voice data, converts it to a voice pattern, and registers the pattern with the registration number.
- If a syntax number or reject value is specified, these are set in the registration number table.
- If omitted, 0 and 0FEH are respectively assumed for the syntax number and reject value.

Status output : 00H (normal completion)
09H (command format error)
05H (specified syntax does not exist)
04H (level adjust not performed)
03H (voice too long)
0BH (voice too short)

3.3.3 Recognition

(1) RECOGNITION (2 to 33 bytes)

Format : 03H,[syntax No.],...,[syntax No.],0FFH
00H ≤ syntax No. ≤ 80H
A maximum of 31 syntax numbers can be specified; if omitted, 0 is assumed.

Function : Inputs voice data, compares against the registered voice patterns and outputs the result.

- Analyzes input voice data and converts it to a voice pattern.
- Performs matching calculation of the input word against all registered word patterns with the specified syntax number.
- The result of the matching calculation is output as the registration number of the pattern with the smallest distance from the input word, the distance value, and the status codes (00H or 0AH). These values are output 1 byte at a time to the host system.
- Matching will be performed against all of the registered patterns if a syntax number of 0 is specified.

Status output : 00H (normal completion; followed by output of registration number (1 byte) and distance value (1 byte))
03H (voice too long)
04H (level not adjusted)
05H (specified syntax does not exist)
06H (registered pattern does not exist)
07H (distance value greater than the bank reject value - corresponding pattern does not exist)
09H (command format error)
0BH (voice too short)

0AH (distance value smaller than the bank reject value but greater than the word reject value; followed by output of registration number (1 byte) and distance value (1 byte))

(2) SECOND DECISION (2 bytes)

Format : 04H,0FFH

Function : After the recognition result is output, the registration number and distance value of the registered pattern with the next smallest distance are output to the host system following the status code (00H or 0AH).

° This command is valid only after the RECOGNITION command is executed.

Status output : 00H (normal completion). After this code is output, the registration number and the distance value are output to the host 1 byte at a time.

07H (distance value greater than the bank reject value - second candidate does not exist)

09H (command format error)

0AH (distance value smaller than the bank reject value but greater than the word reject value; followed by output of registration number (1 byte) and distance value (1 byte))

3.3.4 Transfer of pattern data

(1) UP LOAD (2 bytes)

Format : 07H,0FFH

Function : Outputs the registered patterns in the current memory bank to the host system.

- This command is paired with the DOWN LOAD command to save and load registered patterns.

Status : 00H (normal completion)

output 06H (registered pattern does not exist)

09H (command format error)

(2) DOWN LOAD (3 bytes)

Format : 06H,number of patterns,0FFH,pattern list

01H $\leq$ number of patterns $\leq$ 80H

Function : Loads the registered patterns from the host system into the current memory bank.

- Number of patterns indicates the number of patterns to be sent from the host. It is not the registration number.

Status : 00H (normal completion)

output 09H (command format error)

<Note>

If the number of patterns specified as the second parameter of this command is greater than the number of patterns actually sent, the next data sent (next command, etc.) will be read as pattern data.

3.3.5 Test

(1) MEMORY TEST (2 bytes)

Format : 09H,0FFH

Function : Performs a read/write test of all memory banks set by the MM0 and MM1 pins of the μPD7762G.

Status : 00H (normal completion)

output 09H (command format error)

0CH (read/write error)

<Note>

Since this command performs a read/write test of the memory, all registered patterns will be destroyed.

3.3.6 Status codes

Table 3-3 Status Output Code List

00H	Acknowledge	Normal completion
01H	Level over	Input voice level too high
02H	Level under	Input voice level too low
03H	Time over	Voice input longer than two seconds
04H	No adjust	ATC values for the current bank have not been adjusted
05H	No syntax	Corresponding syntax number does not exist
06H	No registration	Registered pattern does not exist
07H	Bank reject over	Distance value greater than the bank reject value
08H	No bank	Specified bank does not exist
09H	Invalid command	Command format error
0AH	Word reject over	Distance value smaller than the bank reject value but greater than the word reject value
0BH	Too short	Voice is too short
0CH	Memory I/O error	Memory test error or hardware I/O error

Note: When execution of the LEVEL ADJUST command is bypassed the result status for this command will not be output.

3.4 Syntax Groups

Syntax groups are set by specifying a syntax number for words when the voice patterns are registered. By specifying a syntax number when recognition is performed, the number of words against which it is necessary for the input voice to be matched can be reduced. The registered vocabulary can also be partitioned.

Example	Tokyo	Los Angeles
	Hong Kong	Paris
	Singapore	London
	New York	Munich

(1) At registration

Set syntax numbers so they correspond to the registration numbers when registering words. In the previous example, the words are divided into three syntax groups: Asia (1), North America (2), and Europe (3).

(2) Recognition

By specifying the syntax group when performing recognition, only those registered words with the specified syntax number will be used as the object for matching calculation and recognition.

To recognize an Asian place-name, specify syntax number 1 and recognition will be performed comparing the input word against registered words "Hong Kong," "Tokyo," and "Singapore."

Word	Reg. No.	Syntax No.	
Hong Kong	1	1	Syntax group 1
Singapore	2	1	
Tokyo	3	1	
New York	4	2	Syntax group 2
Los Angeles	5	2	
London	6	3	Syntax group 3
Paris	7	3	
Munich	8	3	

3.5 Reject Values

Recognition is carried out based on a distance value obtained by comparing the input voice pattern with registered voice patterns. The maximum permissible distance value (valid range) for recognition can be set when registering the standard patterns.

Thus recognition will be valid during pattern matching if the distance between the patterns is within the tolerance range specified by the reject value.

The result will then be output as the registration number and distance value of the word with the smallest distance value from the input voice pattern.

If the distance between patterns is greater than the reject value, the result will be invalid and output as an error code.

Two kinds of reject values can be set: the bank reject value, which is set for each memory bank, and the word reject value, which is set for each registered word. Recognition will be performed based on the smaller of the two values.

When a large distance value is expected, a large reject value should be set for that word. This will improve the recognition rate.

Example

Word	Bank No.	Word reject value	Bank reject value	Effective reject value
a	0	6	7	6
b	0	8	7	7
c	0	9	7	7
d	1	6	8	6
e	1	8	8	8
f	1	9	8	8

3.6 Parameters for UP LOAD and DOWN LOAD commands

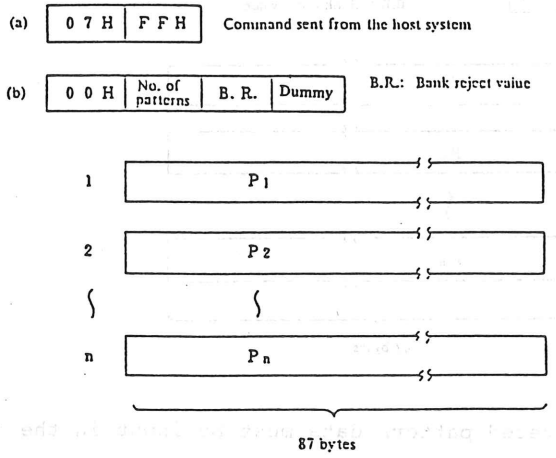
Use the UP LOAD and DOWN LOAD commands to transfer registered patterns between the recognition system and the host system.

(1) UP LOAD (Recognition system → host system)

(a) Send an UP LOAD command from the host system

(b) The recognition system responds with 00H (acknowledge) code and then outputs the number of patterns, bank reject value, and dummy data. This data transfer is performed in byte units. Finally, the recognition system outputs the registered pattern data (87 bytes per word) in the order of registration number, syntax number, word reject value, and pattern data.

Assuming n as the number of patterns, use this formula to find the number of bytes of data sent from the recognition system:
(3+87·n) bytes

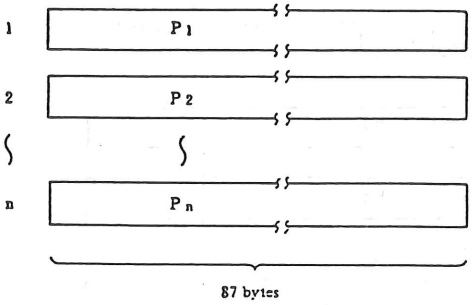


(2) DOWN LOAD (Host system → recognition system)
(a) DOWN LOAD command is sent from the host system.
(b) The recognition system outputs an 00H (acknowledge) code.
(c) The host system sends the bank reject value and dummy data (1 byte each), followed by the pattern data (87 bytes per word).
Assuming n as the number of patterns, use this formula to find the total bytes sent from the host:
(2+87·n) bytes
(d) The recognition system outputs 00H (acknowledge) code.

(a) | 0 6 H | No. of patterns | F F H | Command sent from host system

(b) | 0 0 H | Acknowledge code sent from recognition system

(c) | B.R. | Dummy | B.R.: Bank reject value



* The registered pattern data must be input in the same format as that output by the recognition system.

CHAPTER 4 OPERATION EXAMPLES

This chapter provides program examples for data handlers and command operations of the host system. Although program details may vary depending on the host system, the same method is employed for all systems.

4.1 Standard Operation

These two commands are essential for voice recognition operation.

(1) TRAINING

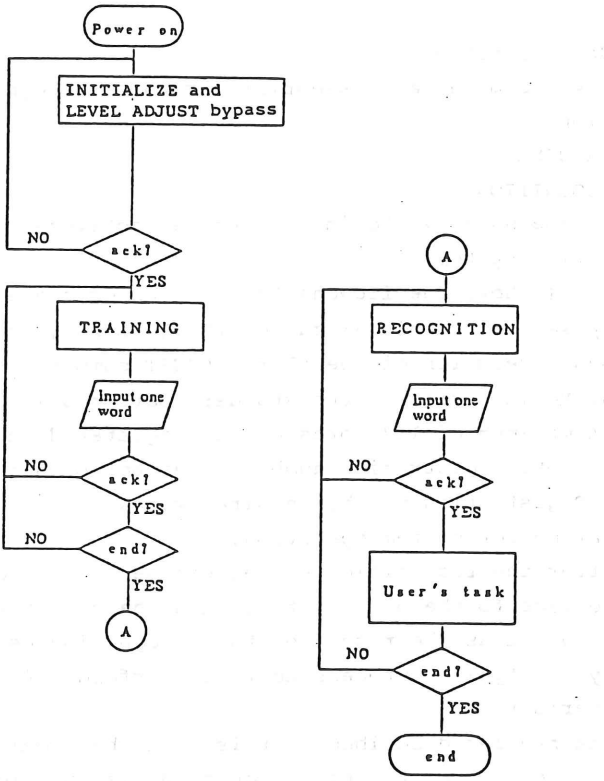
(2) RECOGNITION

Other commands serve to improve the effectiveness of the recognition system.

Figure 4-1 shows the flowcharts for each of these commands. After power ON or initialization (INITIALIZE), processing to bypass execution of the LEVEL ADJUST command is performed. Registration of the standard patterns is performed next. A maximum of 128 words can be registered in each memory bank. Registration numbers need not be assigned in order. Registration of the required words is the final preparation for system operation.

Thereafter the recognition system can be used as an input device to the host system, with the registration number output as the result of the recognition used to specify the type of processing to be performed (see Fig. 4-1, User's tasks).

The data handler described next is used when commands are actually being sent to the recognition system. Fig. 4-2 shows an example of this type of data handler. In it, the voice level is being adjusted. A μPD8085A is assumed to be the host. A different host would require essentially the same procedure, however.



Uppercase letters: Commands

ack: Status code output from the recognition system (Acknowledge code)

Fig. 4-2 Training to Recognition

4.2 Data Handler

This is an example using a μPD8085A for the host system. All routines given below are described in 8085A assembly language.

4.2.1 μPD8255A-5 (Parallel)

Mount a μPD8255A-5 as a peripheral device of the host system. The host performs initialization and other operations.

Fig. 4-2 shows the initialization procedure for the μPD8255A-5; Fig. 4-3 shows the data I/O procedure; and Fig. 4-4 shows program examples for each operation (initialize (a), data output (b), and data input (c)). These handlers all check the state (OBF,IBF) of port C of the μPD8255A-5 by software to realize data transfer using bidirectional handlers.

4.2.2 μPD8251AF (RS-232C)

μPD8251AFs are placed in both the host and the recognition systems. Data transfer is performed between these interfaces.

Fig. 4-5 shows the initialization procedure for the μPD8251A; Fig. 4-6 shows the I/O procedure example; and Fig. 4-7 shows the program examples for each procedure (initialization (a), data output (b), and data input (c)).

All these handlers check the status data of the μPD8251AF by software.

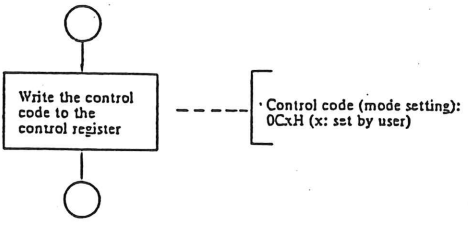


Fig. 4-2 μPD8255 Initialization Procedure

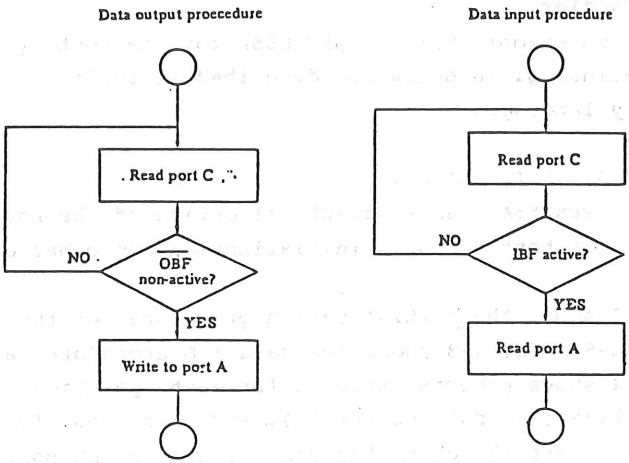


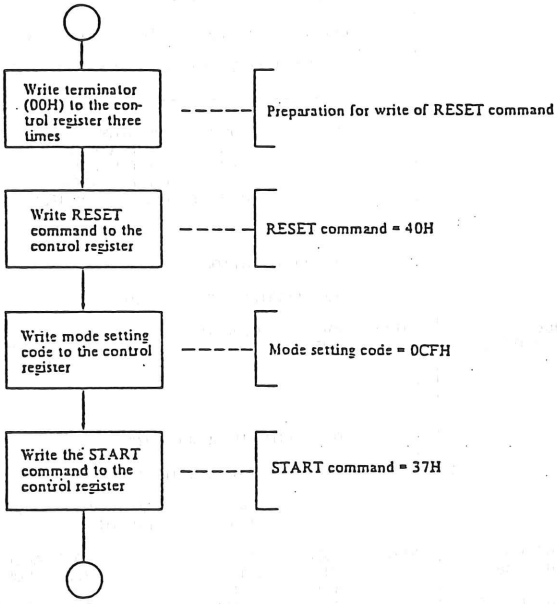
Fig. 4-3 μPD8255 Data I/O Procedure

```
** UCOM-85 ASSEMBLE LIST ** (UPD8255 DATA HANDLER

E STNO ADRS OBJECT M   SOURCE STATEMENTS

  0002                  ;-----------------------------------------------
  0003                  ;
  0004                  ;   SPEECH RECOGNITION SYSTEM  DATA  HANDLER
  0005                  ;
  0006                  ;       FOR UPD8255  BY  UPD8085AC/D ASSEMBLER
  0007                  ;
  0008                  ;-----------------------------------------------
  0009                  ;
  0010                  ;       UPD8255  ADDRESS  ASSIGN
  0011                  ;                80H  :  PORT-A ADDRESS
  0012                  ;                81H  :  PORT-B ADDRESS
  0013                  ;                82H  :  PORT-C ADDRESS
  0014                  ;                83H  :  CONTROL ADDRESS
  0015                  ;
  0016                  ;-----------------------------------------------
  0017                  ;
  0018                  ;       INITIALIZATION OF UPD8255
  0019                  ;
  0020                  ;       I/O CONDITION    :  NOTHING
  0021                  ;
  0022 0000 3EC2    a   INIT:   MVI     A,0C2H          ;0C2H = MODE 2
  0023 0002 D383        INIT:   OUT     83H             ;83H = CONTROL
  0024 0004 C9          INIT:   RET                     ;RETURN
  0025                  ;
  0026                  ;
  0027                  ;
  0028                  ;       DATA OUTPUT SUBROUTINE
  0029                  ;
  0030              b   ;               I/O  CONDITION
  0031                  ;
  0032                  ;               INPUT    :  ACC = OUTPUT DATA
  0033                  ;               OUTPUT   :  NOTHING
  0034                  ;
  0035 0005 F5      DOUT:   PUSH    PSW             ;SAVE ACCUMULATOR
  0036 0006 DB82            IN      82H             ;82H = PORT-C
  0037 0008 E680            ANI     80H             ;80H = MASK DATA
  0038 000A CA0600          JZ      DOUT+1          ;OBF STATUS CHECK
  0039 000D F1              POP     PSW             ;RESTORE ACCUMULATOR
  0040 000E D380            OUT     80H             ;80H = PORT-A
  0041 0010 C9              RET                     ;RETURN
  0042                  ;
  0043                  ;
  0044                  ;       DATA INPUT SUBROUTINE
  0045                  ;
  0046                  ;               I/O CONDITION
  0047                  ;
  0048              c   ;               INPUT    :  NOTHING
  0049                  ;               OUTPUE   :  ACC = RETURN CODE
  0050                  ;
  0051 0011 DB82    DINP:   IN      82H             ;82H = PORT-C
  0052 0013 E620            ANI     20H             ;20H = MASK DATA
  0053 0015 CA1100          JZ      DINP            ;IBF STATUS CHECK
  0054 0018 DB80            IN      80H             ;80H = PORT-A
  0055 001A C9              RET                     ;RETURN
  0056                  ;
  0057                  ;
  0058 0000                 END
```

Fig. 4-4 μPD8255A-5 Data Handler Program Example


Write terminator (00H) to the control register three times
Preparation for write of RESET command
Write RESET command to the control register
RESET command = 40H
Write mode setting code to the control register
Mode setting code = 0CFH
Write the START command to the control register
START command = 37H

NOTE: In this flowchart, use is assumed of μPD8251AFs at both the host system and the recognition system.

Fig. 4-5 μPD8251AF Initialization Procedure

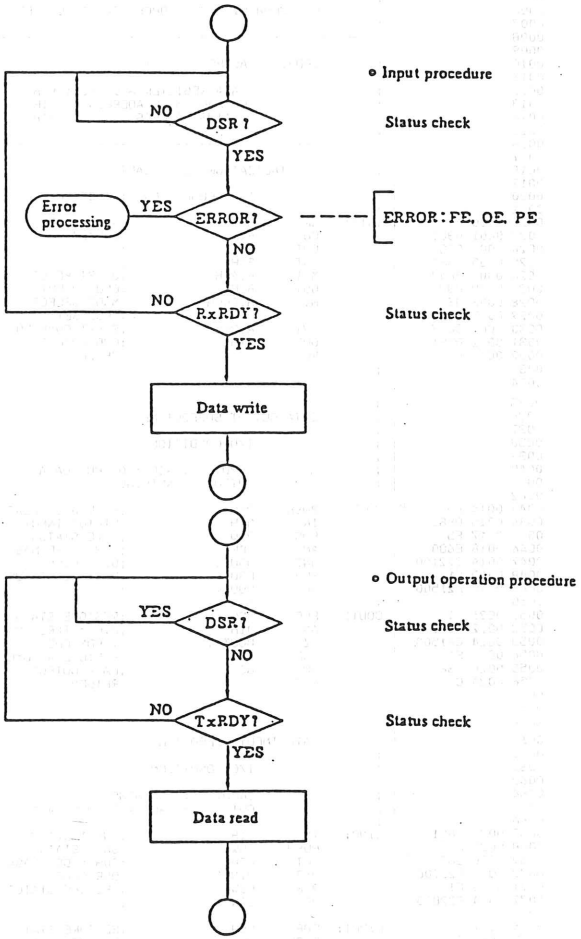


Fig. 4-6 μPD8251AF I/O Operation Procedure

```
** UCOM-85 ASSEMBLE LIST ** (UPD8251 DATA HANDLER

E STNO ADRS OBJECT M   SOURCE STATEMENTS

  0002                 ;-------------------------------------------------------
  0003                 ;
  0004                 ;   SPEECH RECOGNITION SYSTEM DATA HANDLER
  0005                 ;
  0006                 ;       FOR UPD8251  BY  UPD8085AC/D ASSEMBLER
  0007                 ;
  0008                 ;-------------------------------------------------------
  0009                 ;
  0010                 ;       UPD8251  ADDRESS  ASSIGN
  0011                 ;
  0012                 ;               DATA REGISTER ADDRESS : 80H
  0013                 ;               COMMAND/MODE ADDRESS  : 81H
  0014                 ;               STATUS  ADDRESS       : 81H
  0015                 ;
  0016                 ;-------------------------------------------------------
  0017                 ;
  0018                 ;       INITIALIZATION  OF  USART
  0019                 ;
  0020                 ;               I/O  CONDITION  :  NOTHING
  0021                 ;
  0022 0000 AF         INIT:   XRA     A               ;ACC CLEAR
  0023 0001 D381               OUT     81H             ;DUMMEY
  0024 0003 D381               OUT     81H             ;
  0025 0005 D381   a           OUT     81H             ;
  0026 0007 3E40               MVI     A,40H           ;USART RESET
  0027 0009 D381               OUT     81H             ;CMD OUTPUT
  0028 000B 3ECF               MVI     A,0CFH          ;MODE SELECT
  0029 000D D381               OUT     81H             ;MODE SET
  0030 000F 3E37               MVI     A,37H           ;START COMMAND
  0031 0011 D381               OUT     81H             ;CMD OUTPUT
  0032 0013 C9                 RET                     ;RETURN
  0033                 ;
  0034                 ;
  0035                 ;
  0036                 ;       DATA OUTPUT SUBROUTINE
  0037                 ;
  0038                 ;               I/O CONDITION
  0039                 ;
  0040                 ;               INPUT   : ACC = OUTPUT DATA
  0041                 ;               OUTPUT  : NOTHING
  0042                 ;
  0043 0014 F5     b   DOUT:   PUSH    PSW             ;SAVE ACCUMULATOR
  0044 0015 DB81               IN      81H             ;STATUS INPUT
  0045 0017 F5                 PUSH    PSW             ;SAVE STATUS
  0046 0018 E680               ANI     80H             ;80H = DSR MASK
  0047 001A C22100             JNZ     DOUT1           ;DSR CHECK
  0048 001D F1                 POP     PSW             ;RESTORE STATUS
  0049 001E F21500             JP      DOUT+1          ;
  0050                 ;
  0051 0021 F1         DOUT1:  POP     PSW             ;RESTORE STATUS
  0052 0022 E601               ANI     01H             ;01H = TXRDY MASK
  0053 0024 CA1500             JZ      DOUT+1          ;TXRDY CHECK
  0054 0027 F1                 POP     PSW             ;RESTORE ACCUMULATOR
  0055 0028 D380               OUT     80H             ;DATA OUTPUT
  0056 002A C9                 RET                     ;RETURN
  0057                 ;
  0058                 ;
  0059                 ;
  0060                 ;       DATA INPUT SUBROUTINE
  0061                 ;
  0062                 ;               I/O CONDITION
  0063                 ;
  0064                 ;               INPUT   :  NOTHING
  0065                 ;               OUTPUT  :  ACC = RETURN DATA
  0066                 ;
  0067 002B DB81       DINP:   IN      81H             ;INPUT STATUS
  0068 002D F5     c           PUSH    PSW             ;SAVE STATUS
  0069 002E E680               ANI     80H             ;80H = DSR MASK
  0070 0030 C23700             JNZ     DINP1           ;DSR CHECK
  0071 0033 F1                 POP     PSW             ;RESTORE STATUS
  0072 0034 F22B00             JP      DINP            ;
  0073                 ;
  0074 0037 F1         DINP1:  POP     PSW             ;RESTORE STATUS
  0075 0038 F5                 PUSH    PSW             ;RESAVE STATUS
  0076 0039 E638               ANI     38H             ;38H = ERROR MASK
  0077 003B C24700             JNZ     IOERR           ;ERROR CHECK
  0078 003E F1                 POP     PSW             ;RESTORE STATUS
  0079 003F E602               ANI     02H             ;02H = RXRDY MASK
  0080 0041 CA2B00             JZ      DINP            ;RXRDY CHECK
  0081 0044 DB80               IN      80H             ;INPUT RET CODE
  0082 0046 C9                 RET                     ;RETURN
  0083                 ;
  0084 0047 00         IOERR:  NOP
  0085                 ;
  0086 0000                    END
```

Fig. 4-7 µPD8251AF Data Handler Example

4.3 Command Application Examples

Commands requiring cautions about their application are shown in Figs. 4-8 to 4-11.

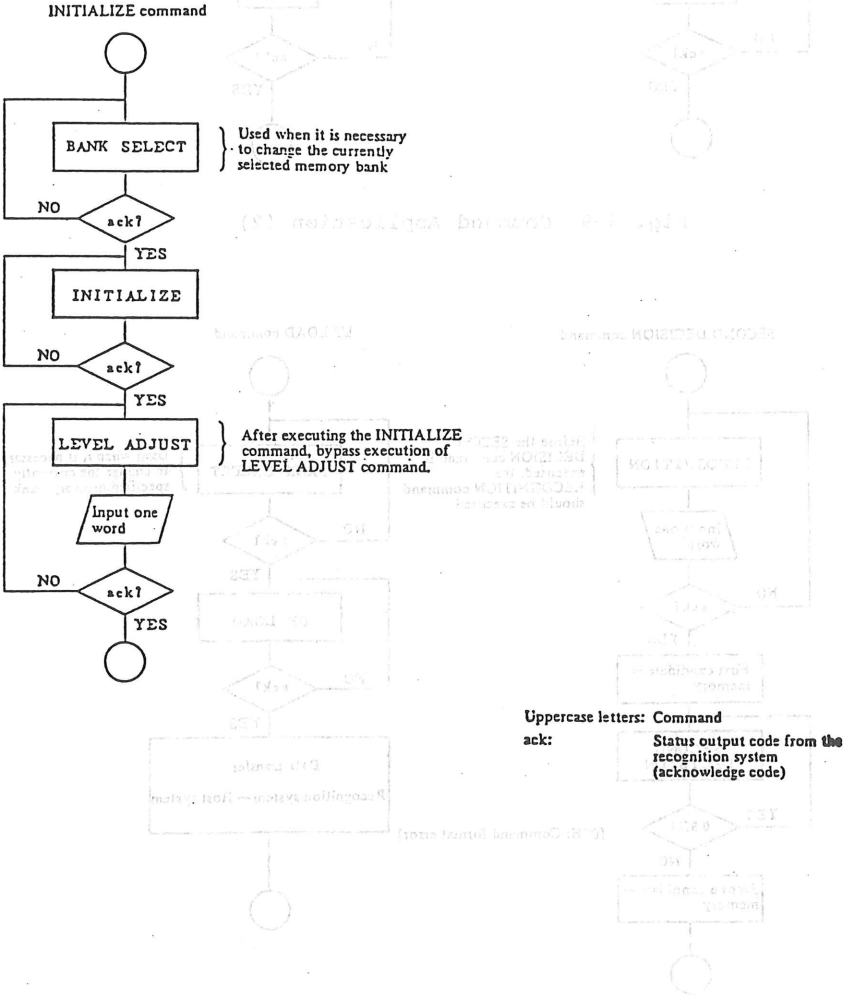


Fig. 4-8 Command Application (1)

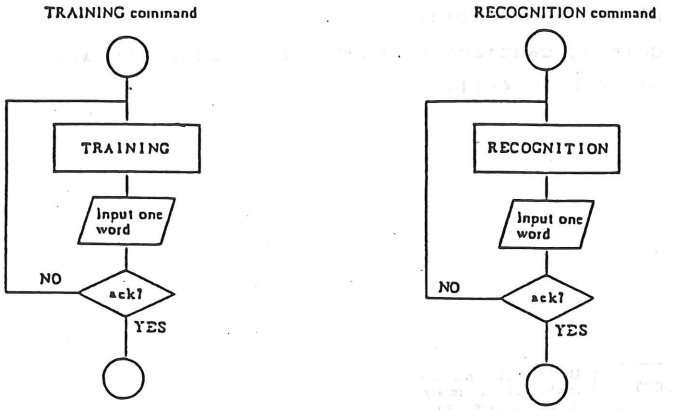


Fig. 4-9 Command Application (2)

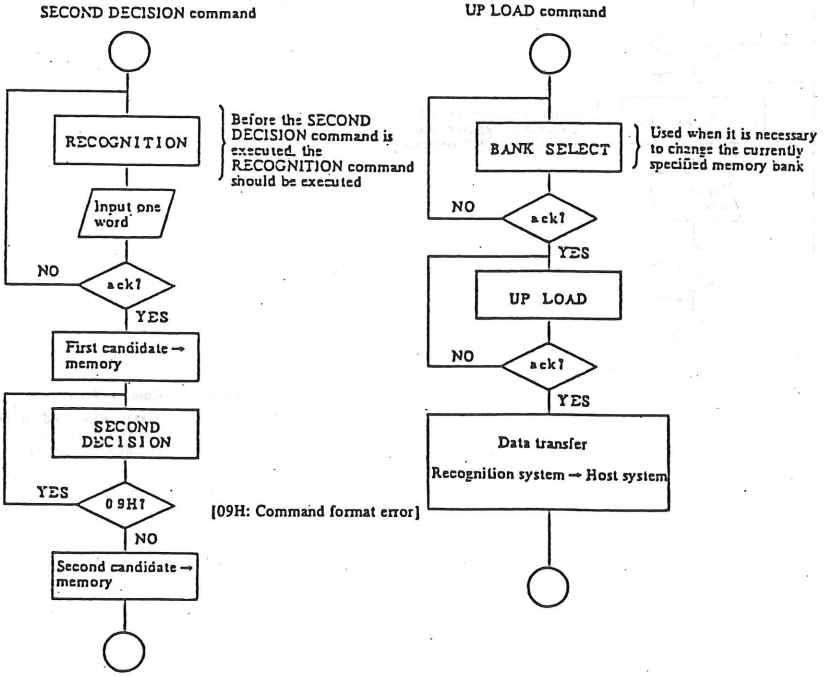


Fig. 4-10 Command Application (3)

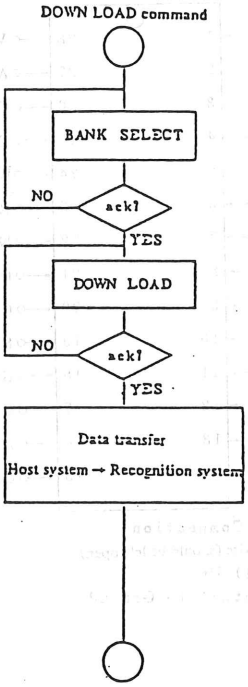
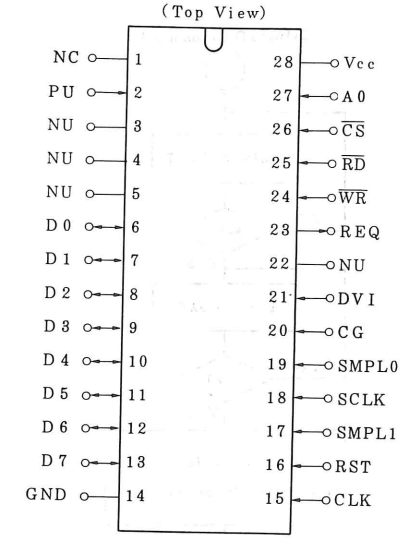


Fig. 4-11 Command Application Example (4)

APPENDIX A

Pin Connections of the Voice Recognition LSI Set

A.1 μPD7761D



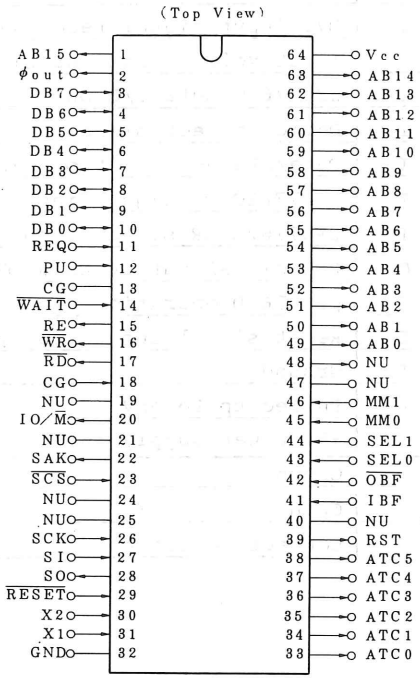
NC : No Connection
NU : No Use (should be left open)
PU : Pull Up
CG : Contact to Ground

Fig. A-1 μPD7761D Pin Connections

Table A-1 μPD7761D Pin Functions

Terminal	I/O	Function
DVI	I	MC-4760 DVO signal input
SCLCK	I	DVI input signal read timing clock input
SMPL0,1	I	Input voice signal sampling clock input
D0 to D7	I/O	μPD7762G data I/O bus
CS	I	Device select signal input
A0	I	Data/status selection signal input
RD	I	μPD7762G RD signal input
WR	I	μPD7762G WR signal input
REQ	O	REQ signal output to μPD7762G
CLK	I	μPD7761D operation clock input
RST	I	Reset signal input from μPD7762G
CG	I	Ground
PU	I	Pulled up to +5V
V_{CC}		+5V power supply input
GND		Ground
NU		Open
CG		Connect to ground

A.2 μPD7762G



NU : No Use (should be left open)
PU : Pull Up
CG : Contact to Ground

Fig. A-2 μPD7762G Pin Connections

Table A-2 μPD7762G Pin Functions

Terminal	I/O	Function
B0 to B15	O	Address bus
B0 to B7	I/O	Data bus
O/M	O	I/O and memory identifying signal output
RD	O	Read signal output
WR	O	Write signal output
M0,1	I	Registered pattern memory capacity specification inputs
RE	O	Refresh control signal output
WAIT	I	Wait signal input
SEL0,1	I	Host interface specification input
OBF	I	μPD8255A-5 OBF signal input
IBF	I	μPD8255A-5 IBF signal input
SCS	I	Chip select signal input (when using the serial port
SCK	I	Serial port I/O clock signal input
SI	I	Serial data input
SO	O	Serial data output
SAK	O	Serial input acknowledge signal output
REQ	I	μPD7761D REQ signal input
RST	O	μPD7761D reset signal output
X1,2	I	μPD7762G operation clock input
ϕ out	O	Clock output
HST	I	Hot start signal input
RESET	I	RESET signal input
CG	I	Connect to ground
V_{CC}		+V power supply
GND		Ground
NU		Open
PU	I	Pull up to +5V

APPENDIX B
Application Circuit Example

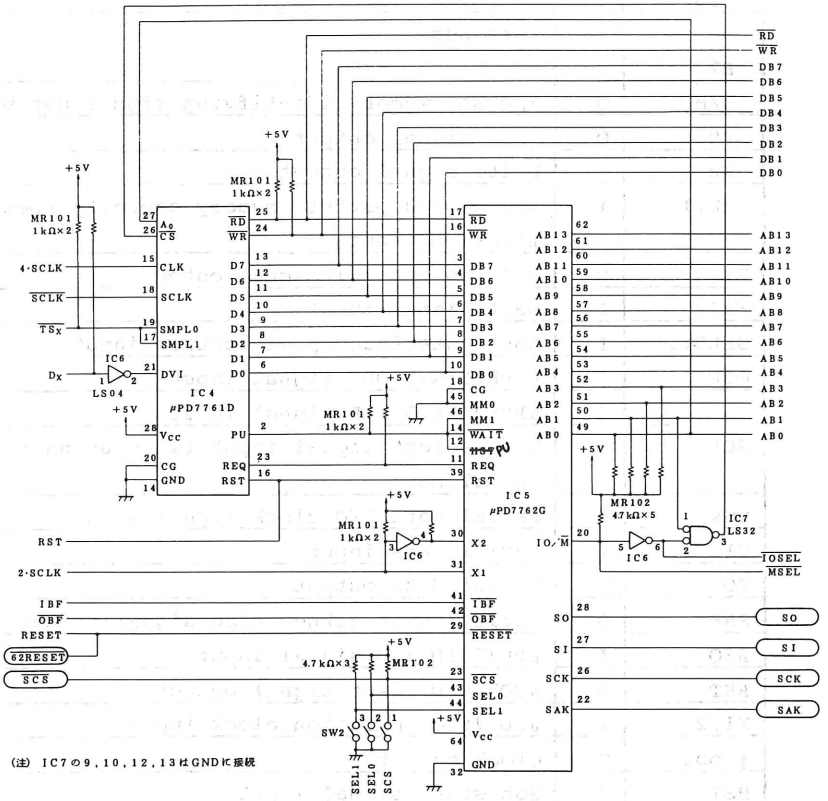


Fig. B-1 Circuit Example for the Voice Recognition LSI Set

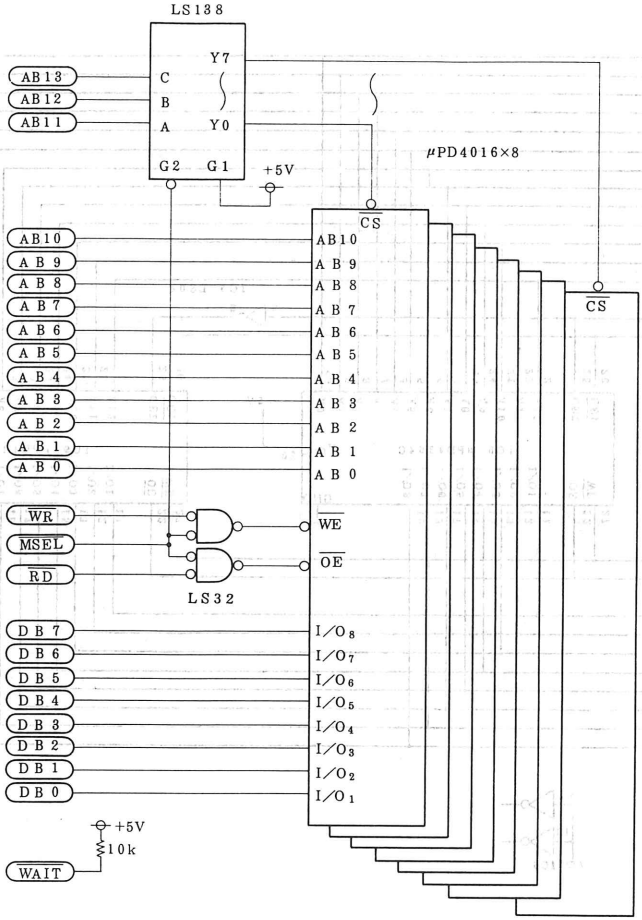


Fig. B-2 Memory Circuit Using Static RAMs μPD4016

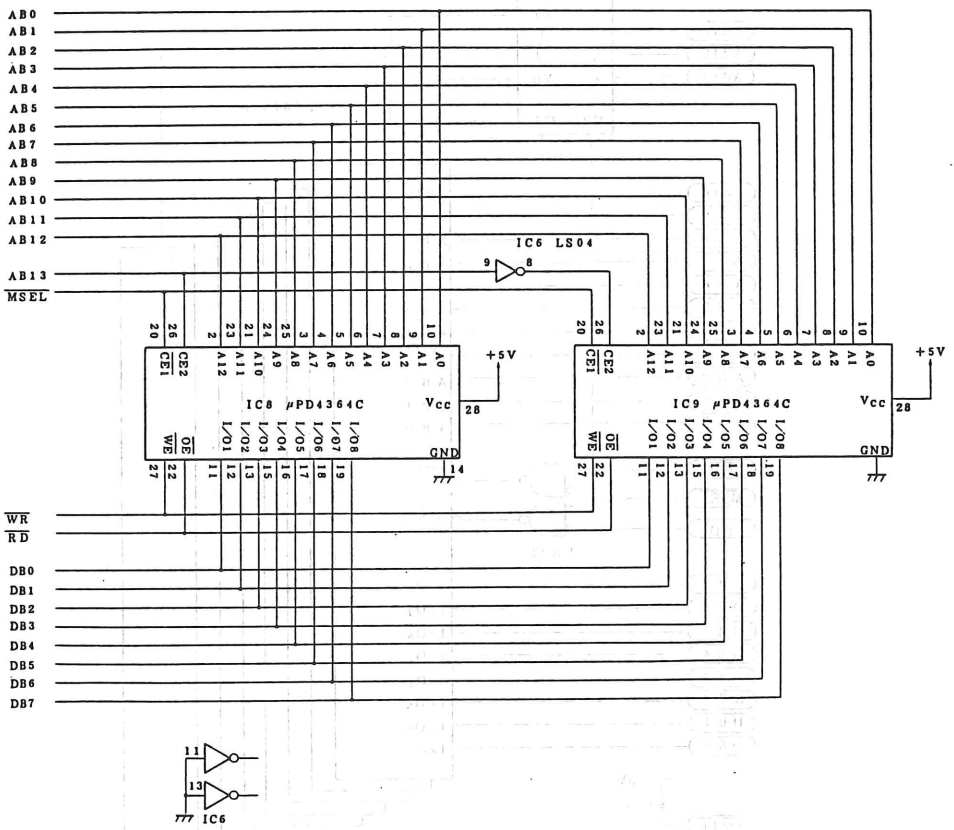
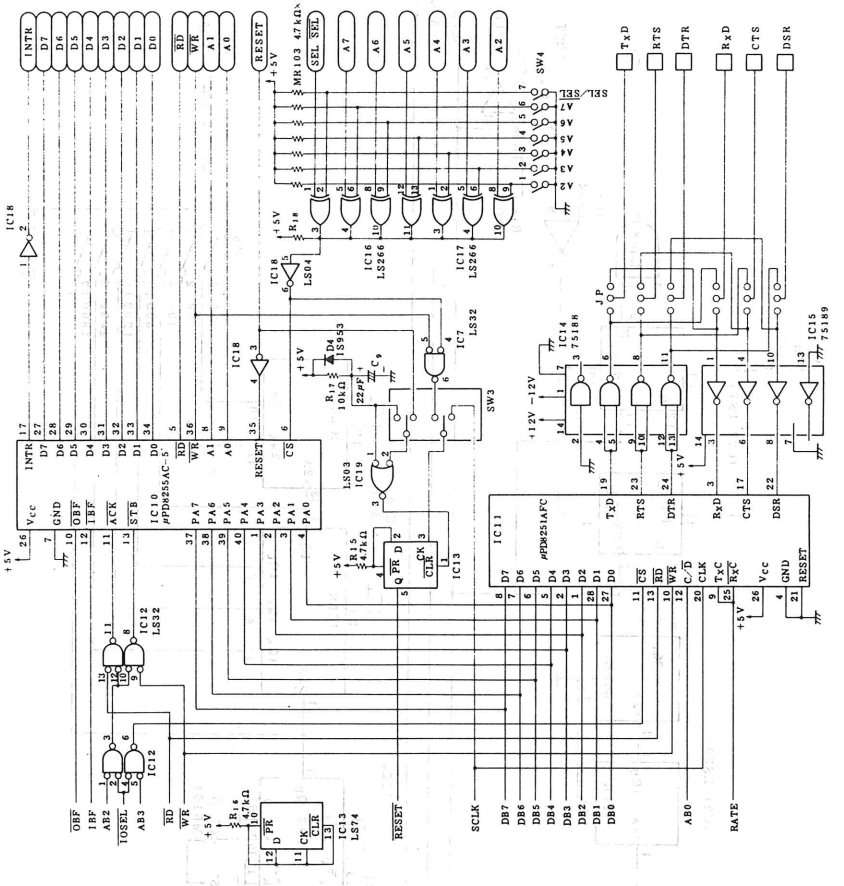


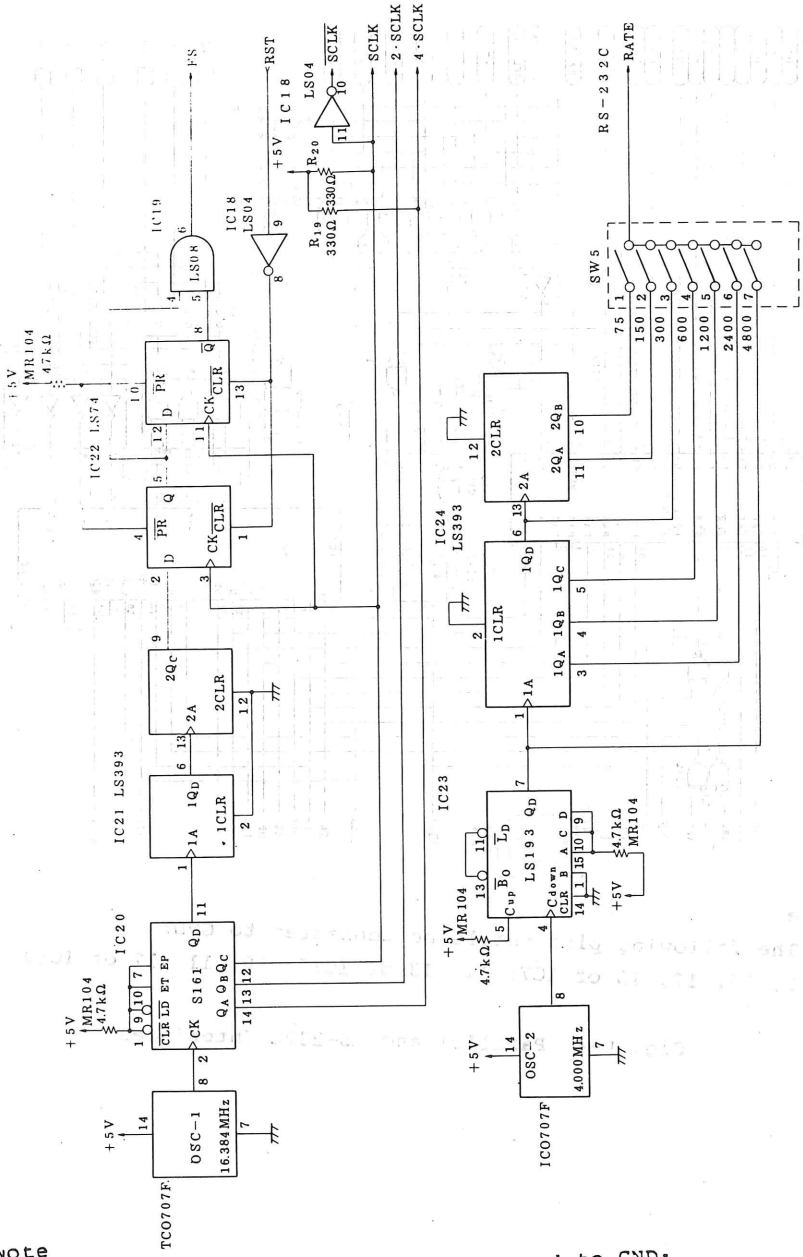
Fig. B-3 Memory Configuration Using Static RAMS (μPD4346C (64K bit))



Note

The following pins should be connected to GND:
9, 10, 12, 13 of IC7; 12, 13 of IC17; 10, 11, 12 of IC13

Fig. B-4 Parallel and RS-232C Interfaces



Note

The following pins should be connected to GND:

13 of IC18; 9, 10, 11, 12, 13 of IC19

OSC-1,OSC-2:CRYSTAL OSCILLATOR

Fig. B-5 Clock Generating Circuit

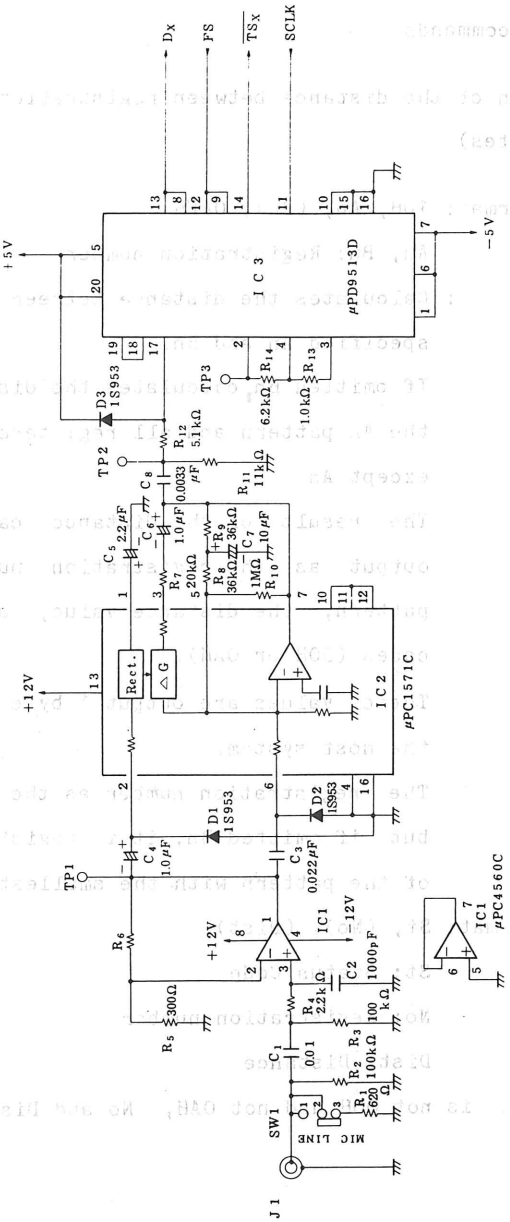


Fig. B-6 Analog Interface

1. Additional commands

1.1 Calculation of the distance between registration patterns (3 to 4 bytes)

Command format: 10H, An, (Bn), OFFH

An, Bn: Registration number

Function : Calculates the distance between patterns specified An and Bn.

If omitted Bn, calculates the distance between the An pattern and all registered patterns except An.

The result of the distance calculation is output as the registration number of the pattern, the distance value, and the status codes (OOH or OAH).

These values are output 1 byte at a time to the host system.

The registration number as the result is Bn, but if omitted Bn, it is registration number of the pattern with the smallest distance.

Output Format: St, (No), (Dist)

St: Status Code

No: Registration number

Dist: Distance

* When St is not OOH and not OAH, No and Dist are blank spaces.

status code: 00H: Normal complete.

00H: Registered pattern does not exist.

07H: Overflow as the result or distance value greater than the bank reject value.

09H: Command forward error

0AH: Distance value greater than the word reject value.

1.2 Cancel of the registration patterns (3 bytes)

Command format: 11H, Registration No., 0FFH

Function : Cancel out the pattern with the registration number from the table.

output format : St

St: Status code

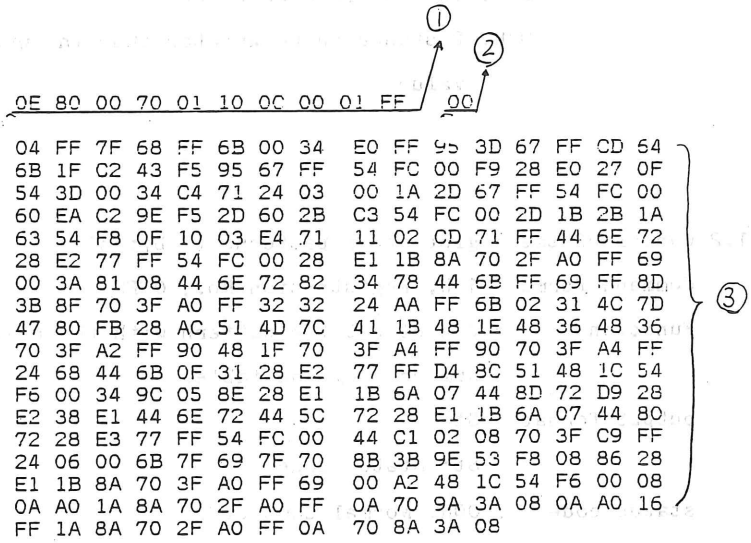
status code : 00H: Normal complete.

06H: Registered pattern does not exist.

09H: Command format error

2. The method to load additional commands program

The additional commands program must be laoded from the host system to the recognition system by the following format.



Notes)

1) Transfer dataformat ①.

2) Accept the status code ②.

3) Transfer data format ③.

3. The method to use additional commands

Process

1) Load the additional commands program to the recognition system, when the recognition system is set up. If not switch off after loading the program, these commands can have been used.

2) Transfer 'execute' command from the host system.

3) Confirm that the status code for 'execute' command is 00H (Ack.).

4) Transfer an additional command.

5) Accept the status codes for the additional command.

4. The example of operation

```
CMD>
CMD> 0F 80 00 70 01 FF      <-- 'execute' command
RETURN STATUS : 00          <-- comfirm Ack code

CMD> 10 01 FF               <-- Distance calculation command,
RETURN STATUS : 00 06 02    <-- The pattern with the smallest
                                distance of 2 is pattern No.6, and
                                the distance value is 2.

CMD> 0F 80 00 70 01 FF
RETURN STATUS : 00

CMD> 10 01 02 FF            <-- Calculating the distance
RETURN STATUS : 00 02 03    <-- between pattern No.1 and No.2.
                                The pattern  The value is 3.

CMD> 0F 80 00 70 01 FF
RETURN STATUS : 00

CMD> 11 01 FF               <-- Deleting pattern No.1
RETURN STATUS : 00

CMD> 0F 80 00 70 01 FF
RETURN STATUS : 00

CMD> 10 01 02 FF
RETURN STATUS : 06          <-- Not registerd

CMD> 0F 80 00 70 01 FF
RETURN STATUS : 00

CMD> 10 02 FF
RETURN STATUS : 00 06 01

CMD> 0F 80 00 70 01 FF
RETURN STATUS : 00

CMD> 11 06 FF
RETURN STATUS : 00

CMD> 0F 80 00 70 01 FF
RETURN STATUS : 00

CMD> 10 02 FF
RETURN STATUS : 00 05 02

CMD> 04 FF                  <-- Second decision command
RETURN STATUS : 00 08 02    <-- The pattern with the next
                                smallest distance

CMD> 0F 80 00 70 01 FF
RETURN STATUS : 00

CMD> 10 02 03 FF
RETURN STATUS : 00 03 04

CMD> 04 FF
RETURN STATUS : 07
```

Note) CMD : Prompt of control program for the host system

5. The environment to use the additional commands

The recognition system by means of speech recognition LSI set can be used independently of the kinds of its standard pattern RAM.

But when using these commands at least pattern memory bank 0 must consist of static RAM. If consisting except static RAM, we cannot guarantee against normal action.

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